



High Definition H.264 MP Encoder

DM6467

Datasheet

Release version	v1.01
Framework	TI (CE)
API	XDM 1.0
Platform	DM6467



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1. Features and Validation

1.1 Description

H.264 encoding is extensively used for achieving good video quality over a wide range of bit-rates at reasonable computational complexity in applications such as video telephony, surveillance and video streaming.

This document covers the features supported by Ittiam's H.264 encoder, along with the performance footprints.

1.2 Features Currently Supported by the Encoder

1.2.1 Toolsets Supported

The H.264 encoder supports the following generic toolsets -

- Compliant with Baseline Profile – Level 1, 1.x, 2, 2.x, 3.x, 4
- Supports Main Profile, Level 1, 1.x, 2, 2.x, 3.x, 4 – Field Pictures and CABAC.
- Supports YUV420, YUV422P raw video input formats with chrominance pixel interleaved.
- Quarter pixel accurate Motion Estimation.
- Configurable in-loop De-blocking filter.
- 16x16 partitions only.
- Variable Bit Rate (VBR) control algorithm targeted towards low delay applications.
- Constant Bit Rate (CBR) control algorithm
- Support for run time changes to Target Bit-rate
- Configurable Source and Target Frame-rates. It further allows on the fly changes to both the Source and the Target Frame-rates.
- Support for Encoding IDR Pictures on Request.
- Supports Stride Based Encoding.
- Supports Spatial Quality Modulation Mode.

1.2.2 Interface

- Compliant with TI's XDM (v1.0) interface

1.3 Validation

The encoder has been validated by running it on the target platform and measuring the resource usage during this process.

The output generated by the encoder is then decoded using a reference H.264 decoder (JM decoder), both to ensure the validity of the encoded stream and to measure the quality of the encoded sequence.

2. Performance and Resource Usage

2.1 Settings Used

The sections below list down the platform configuration used to test and measure the performance of the video encoder:

2.1.1 Clock Settings

Module	Clock Frequency (MHz)
ARM	297
DSP	594
Co-processor	297
DDR	297

Table 2-1 Clock Frequencies of Various Modules

2.1.2 Memory Layout

The sizes of the different types of memory used while measuring the performance of the encoder are given below:

Memory Name	Type	Size
L1P	Program Memory (Internal)	0 KB
L1P Cache	Instruction cache	32 KB
L1D	Data Memory (Internal)	24 KB
L1D Cache	Lowest level Data cache	8 KB
L2	Second level memory	32 KB
L2 Cache	Cache at L2 level	32 KB
DDR	External memory (both program and data)	600 KB

Table 2-2 Memory Configuration used for Performance Benchmarking

Note The performance is highly sensitive to the size of all memory sections except that of DDR. The amount of DDR required depends on the system requirements as well as codec requirements. The DDR Memory requirements shown here exclude framework code/data and buffers requirement to be created while running the codec.

2.2 Resource Usage

2.2.1 Memory Usage

The usage of memory by one instance of encoder is shown below.

Dimension	Code (KB)	External data (KB)		Internal data (KB)		Tables (KB)	Stack (KB)
		Persistent	Scratch	Persistent	Scratch		
1280x720	450	9430	0	-	33	150	10
1920x1088	450	17500	0	-	45	150	10

Table 2-3 Memory Usage for a Single Instance

The following points should be noted about these numbers:

- Input / Output buffers are excluded from external memory numbers
- Internal memory is not used for storing persistent data
- The actual numbers may vary within +/- 5% range.

2.2.2 DMA resource usage

The encoder requires the following resources to properly configure the DMA engine

- 22 EDMA channels.
- 0 QDMA channels.
- 104 PaRAM sets.

2.2.3 I/O buffer memory requirement

The encoder requires the following different pools in the contiguous memory area

Buffer Size (bytes)	Number of Buffers
200	200
1024	10
10240	10
200000	4
500000	4
1234240	3
3258400	3

Table 2-4 Input Output Buffer Requirements

Note The numbers mentioned above are the worst case I/O buffer memory requirement for a standard definition encode. In case of dual core processors (e.g. DM6467) these buffers need to be allocated from the Contiguous Memory Area.

2.3 Encoder Settings

CFG	Frame	Field	Entropy	Quality Mode	De-blocking
CFG_1	√		CABAC	√	√
CFG_2		√	CABAC	√	√

Table 2-5 Configurations used while profiling the encoder

The description of the column headings is contained in the following table.

Toolset	Description
CFG	Configuration – Tool Settings
Frame	Frame Encoding Mode
Field	Field Encoding Mode
Entropy	CABAC Entropy Coding (Main Profile), (CAVLC otherwise)
Quality Mode	Spatial Quality Modulation Mode
De-blocking	In-loop de-blocking filter

Table 2-6 Table explaining what each of the column headings in **Table 2-5** means

Note “√” indicates that the particular tool is enabled during profile.

2.4 Processor Loading

Content				CFG	MCPS	
Sequence	Dimension	FPS	Bit-Rate (kbps)		Average	Peak
Parkrun	1280 x 720	30	6000	CFG_1	265	267
Movie Trailer	1920x1088	24	12000	CFG_1	470	472
Movie Trailer	1920x1088	24	12000	CFG_2	499	501
Riverbed	1920x1088	30	12000	CFG_1	587	589
Riverbed	1920x1088	60	12000	CFG_2	623.7	625.4

Table 2-7 Processor Loading in Terms of Average and Peak MCPS

Note MCPS number quoted here is as measured from the application side including the Codec Engine overheads. Peak MCPS is the maximum average MCPS calculated over a sliding window of 4 pictures. The actual MCPS number may vary within a +/- 2% range. If the Encoder is run in the Interrupt Mode, there is an increase of 8-10% in the MCPS.