

Ittiam HEAAC Decoder

HE-AAC (aacPlus) Decoder

AAC is a popular audio coding technique recommended by MPEG committee. SBR is a tool used in combination with the AAC general audio codec resulting in aacPlus (also known as HEAAC). It provides significant increase in coding gain. In SBR, the high-band, i.e. the high frequency part of the spectrum is replicated using the low-band. The bit-rate is by far below the bit-rate required when using conventional AAC coding. This translates into better quality at lower bit-rates. It can be used in several consumer applications, like mobile streaming and download, digital terrestrial, cable & satellite television broadcasting and Internet Video on demand service.

Features

Features supported:

- MPEG2 and MPEG4 AAC LC (Low complexity), SBR.
- Supports all sampling frequencies & bit rates for AAC only bit-streams.
- Channels: Mono/Stereo/Dual-Mono
- Tools: TNS (Temporal Noise Shaping), PNS (Perceptual Noise Shaping), Intensity Stereo & Mid/Side Stereo
- Bit-streams: ADIF, ADTS, GA Header
- Compliance:
 - ISO/IEC 13818 - 4, 14496 – 4 (MPEG AAC and PNS Conformance)
 - ISO/IEC 14496 - 4:AMD8 (MPEG SBR Conformance)
- Performs Low Power SBR Decoding
- SBR Levels: Level 2 & 3
- For SBR bit-streams supports AAC sampling frequency up to 24/48 kHz (Level 2/3) & SBR sampling frequency up to 48 kHz.
- SBR Signaling: Implicit, hierarchical explicit and backward compatible explicit.
- Supports TI XDMI API
- Robust against erroneous bit-streams
- Optimized for low footprint & processing power
- 16 bit WAV Output format support

Features not supported:

- More than 2 channels of audio.
- SBR Level 4 and 5
- Parametric Stereo Decode
- Channel Coupling
- DRC

Decoder Validation

The MPEG-4 HEAAC decoder implementation has been validated using the latest conformance tool given by MPEG-4.

Resource requirements on C64x Processor

Decode mode	MCPS	Pgm	Tables	Static	Scratch
	Peak	ROM (kB)		RAM (kB)	
SBR Level 2	10.3	122.1	25.2	16.4	9.0

Note: Input/ Output buffers details are given in the next page.

MCPS measurement done on 0 wait-state memory access



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Details of C64x Resources required

CPU Loading

Description	Simulator		Hardware Configuration	
	MCPS	MCPS	MCPS	MCPS
	Ave	Peak	Ave	Peak
AAC	4.6	5.9	11.0	11.5
SBR Level 2	6.9	10.3	14.5	21.3
SBR Level 3	12.2	17.3	25.8	34.1

Memory Usage (kB)

Program	Tables	Static	Scratch	Stack	Input	Output
122.1	25.2	16.4	9.0	2.1	1.5	6.0

Note:

- Performance generated on *CCS 2.20.18 with C64xx Cycle Accurate Simulator with 0 wait state memory access*
- Hardware Configuration performance generated on a DM642 processor with all data and program memory sections placed in the external memory, with cache configuration of 16 kB L1 P Cache, 16 kB D Cache & 64 kB L2 Cache, and cache thrashed after decoding each frame.
- MCPS numbers on the hardware will vary with the I-Cache and D-Cache size and with the memory configuration/placement
- MCPS/MIPS indicate the CPU usage for processing 2 channel music streams (AAC, al05_48.adts 48 kHz, 128 kbps, without TNS), (SBR Level 2, al_sbr_sr_48_2_fsaac24.adts 48 kHz, 48 kbps), (SBR Level 3 al_sbr_sr_48_2_fsaac48.adts, 48 kHz, 48 kbps) .
- Program memory doesn't include the code size of the test bench and standard library functions
- Data memory should be aligned to desired byte-boundary to meet the performance/functionality requirement

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