

Ittiam HEAAC v2 Decoder

HE-AAC v2 (Enhanced aacPlus) Decoder

AAC is a popular audio coding technique recommended by MPEG committee. SBR and PS are the tools used in combination with the AAC general audio codec resulting in Enhanced aacPlus (also known as HEAAC v2). It provides significant increase in coding gain. In SBR, the high-band, i.e. the high frequency part of the spectrum is replicated using the low-band. The bit-rate is by far below the bit-rate required when using conventional AAC coding. This translates into better quality at lower bit-rates. It can be used in consumer applications like mobile streaming and download, digital terrestrial, cable & satellite television broadcasting and Internet Video on demand service.

Features

- MPEG2 and MPEG4 AAC LC (Low complexity), SBR, PS.
- Supports all sampling frequencies & bit rates for AAC only bit-streams.
- Channels: Mono/Stereo/Dual-Mono
- Tools: TNS (Temporal Noise Shaping), PNS (Perceptual Noise Shaping), Intensity Stereo & Mid/Side Stereo
- Bit-streams: ADIF, ADTS, GA Header
- Compliance:
 - ISO/IEC 13818 - 4, 14496 – 4 (MPEG AAC and PNS Conformance)
 - ISO/IEC 14496 - 4:AMD8 (MPEG SBR Conformance)
 - ISO/IEC 14496 – 4:AMD11 (MPEG PS Conformance)
 - ETSI TS 126 406 V6.3.0 (3GPP PS Conformance)
- Performs Low Power SBR Decoding for stereo bit-stream and performs High Quality SBR Decoding for mono or PS bit-stream
- SBR Levels: Level 2 & 3
- For SBR bit-streams supports AAC sampling frequency up to 24/48 kHz (Level 2/3) & SBR sampling frequency up to 48 kHz.

- SBR Signaling: Implicit, hierarchical explicit and backward compatible explicit.
- Supports TI XDMI API
- Robust against erroneous bit-streams
- Optimized for low footprint & processing power
- 16 bit WAV Output format support

Features not supported:

- More than 2 channels of audio.
- SBR Level 4 and 5
- Channel Coupling
- DRC

Decoder Validation

The MPEG-4 HEAAC v2 decoder implementation has been validated using the latest conformance tool given by MPEG-4.

Resource requirements on C64x+ Processor

Decoder mode	MCPS	Pgm	Tables	Static	Scratch
	Peak	ROM (kB)		RAM (kB)	
3GP-PS	9.4	128.0	29.5	22.9	16.0

Note: Input/ Output buffers details are given in the next page.

MCPS measurement done on 0 wait-state memory access



Kane Computing Ltd
 7 Theatre Court, London Road,
 Northwich, Cheshire, CW9 5HB, UK.
 Tel: +44(0)1606 351006
 Fax: +44(0)1606 351007/8
 Email: sales@kanecomputing.com
 Web: www.kanecomputing.co.uk

Details of C64x+ Resources required

CPU Loading

Description	Simulator		Hardware Configuration	
	MCPS	MCPS	MCPS	MCPS
	Ave	Peak	Ave	Peak
AAC	4.3	5.2	8.2	8.7
SBR Level 2	6.2	9.1	11.3	15.3
SBR Level 3	10.6	14.8	20.3	26.3
PS	5.7	8.3	12.1	17.3
3GP-PS	8.3	9.4	17.4	18.6

Memory Usage (kB)

Program	Tables	Static	Scratch	Stack	Input	Output
128.0	29.5	22.9	16.0	2.8	1.5	8.0

Note:

- Simulator performance generated on CCS 3.2.39.5 with C64x+ Cycle Accurate Simulator with 0 wait state memory access
- Hardware Configuration performance generated on a DM6446 processor with all data and program memory sections placed in the external memory, with cache configuration of 32 kB L1 P Cache, 16 kB L1 D Cache & 64 kB L2 Cache, and cache thrashed after decoding each frame.
- MCPS numbers on the hardware will vary with the I-Cache and D-Cache size and with the memory configuration/placement
- MCPS/MIPS indicate the CPU usage for processing 2 channel music streams (AAC, al05_48.adts 48 kHz, 128 kbps, without TNS), (SBR Level 2, al_sbr_sr_48_2_fsaac24.adts 48 kHz, 48 kbps), (SBR Level 3 al_sbr_sr_48_2_fsaac48.adts, 48 kHz, 48 kbps), (PS al_sbr_ps_iid_34_4.adts, 48 kHz, 32 kbps) and (3GP-PS s_cl_2t_1_28s.adts, 48 kHz, 28 kbps).
- Program memory doesn't include the code size of the test bench and standard library functions
- Data memory should be aligned to desired byte-boundary to meet the performance/functionality requirement

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