

Ittiam MP3 Decoder

MP3 Decoder

MPEG-2/MP3 audio coding (also known as MPEG-2 BC) is a coding technique used on audio signals sampled in the range of 16 kilohertz (kHz) to 48 (kHz). The standard is backward compatible with the MPEG-1 MP3 and supports decoding of three layers. The decoder operates on a frame of 1152 samples (Layers 2 and 3) or 384 samples (Layer 1). It supports bit-rates from 8 to 320 (Layer 3), 8 to 384 (Layer 2) and 32 to 448 (Layer 1) kbps (depending on the sampling rate).

Features

- Decoding of MPEG-1 & 2 Layer 1, 2, 3 bit-streams.
- Decoder is Full Accuracy ISO/IEC 11172-3 audio decoder.
- Supports bit-rates
 - 32-320/8-160 (MPEG1/MPEG2) kbps for Layer3.
 - 32-384/8-160 (MPEG1/MPEG2) kbps for Layer2.
 - 32-448/32-256 (MPEG1/MPEG2) kbps for Layer1.
- Supports all sample rates from 16 kHz to 48 kHz.
- Supports free format bit-rate decoding for Layer3.
- Mono/Stereo channels and Joint stereo.
- Supports TI XDMI Interface.
- Multi-channel reentrant software.
- The implementation has been tested on a variety bitstreams and audio files for robustness and quality.
- Optimized for low footprint and processing power.

Decoder Validation

The MP3 decoder implementation has been tested for conformance against the MP3 Test specification (as defined in the ISO-11172-4 and ISO-13818-4 test specification). The decoder has also been tested for robustness against bitstream errors and quality based on listening tests.

Resource requirements on C64x+ Processor

Function	MCPS	Pgm	Tables	Static	Scratch
	Peak	ROM (kB)		RAM (kB)	
Decode	7.0	44.7	11.6	12.4	7.0

Note: Input/ Output buffers details are given in the next page.

MCPS/MIPS indicate the CPU usage for processing Stereo 128kbps, 44.1 kHz worst case stream.

MIPS for MCPS measurement on 0 wait-state memory access



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Details of C64x+ Resources required

CPU Loading

Description	Simulator		Hardware Configuration	
	MCPS	MCPS	MCPS	MCPS
	Ave	Peak	Ave	Peak
Layer 3 decode 128kbps. 44.1kHz	6.1	7.0	9.0	10.4
Layer 3 decode 320kbps, 48kHz	8.8	10.5	12.2	14.3

Memory Usage (kB)

Program	Tables	Stack	Static	Scratch	Input	Output
44.7	11.6	<1	12.4	7.0	2.0	4.5

Note:

- Simulator performance generated on *CCS 3.2.39.5 with C64x+ Cycle Accurate Simulator with 0 wait state memory access*
- Hardware Configuration performance generated on a DM6446 processor with all data and program memory sections placed in the external memory, with cache configuration of 32 kB L1 P Cache, 16 kB L1 D Cache & 64 kB L2 Cache, and cache thrashed after decoding each frame.
- MCPS numbers on the hardware will vary with the I-Cache and D-Cache size and with the memory configuration/placement
- Both the 128 kbps and the 320 kbps testvectors were generated using *hihat.wav*
- Program memory doesn't include the code size of the test bench and standard library functions
- Data memory should be aligned to desired byte-boundary to meet the performance/functionality requirement

Notice

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