

Ittiam MPEG2 Layer 2 Encoder

MPEG Layer 2 Encoder

MPEG-2 Layer 2 Encoder is an audio coding technique used on audio signals sampled at the range of 16 KHz to 48 KHz. The coder operates on frames of length 1152 sample. It generates encoded bit streams at 32-448 Kbps.

This document describes the MCPS and memory requirements for MPEG-2 Layer 2 Encoder on DM642 board.

Features

- The encoder bit stream conforms to the MPEG-1 (ISO/IEC 11172 - 3) and MPEG-2 (ISO/IEC 13818 - 3) standards.
- Sampling Rates 16, 22.05, 24, 32, 44.1, 48 KHz.
- Layer-2: from 32 Kbps to 384 Kbps Constant bit rate.
- Joint Stereo, Dual Channel (Stereo), Single Channel.
- Supports TI XDAIS Interface.
- Optimized for low footprint and processing power.

Resource requirements on C64x Processor

Function	MCPS	Pgm	Tables	Static	Scratch
	Peak	ROM (kb)		RAM (kb)	
MPEG-2 Layer 2 Encoder	17.34	46.2	8.6	9	18.3

Note

Input/ Output buffers details are given in the next page.

MCPS indicate the CPU usage for encoding 2 channel, 44.1kHz input at 192kbps.

MCPS measurement on 0 wait-state memory access



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Details of C64x Resources required

CPU Loading

Description	Simulator		Hardware Configuration	
	MCPS	MCPS	MCPS	MCPS
	Ave	Peak	Ave	Peak
input.wav (2 channel, 44100Hz, 192kbps)	15.29	17.34	20.46	22.47

Memory Usage

Program	Tables	Static	Scratch	Input	Output
46.2	8.6	9	18.3	4.5	1.7

Note:

- I/O Buffers
 - Input Buffer Size : 4.5kbytes
 - Output Buffer Size 1.7kbytes
- Performance generated on *CCS 2.20.18 with C64xx Cycle Accurate Simulator with 0 wait state memory access*
- Hardware Configuration performance generated on a DM642 processor with all data and program memory sections placed in the external memory, with cache configuration of 16 kB L1 P Cache, 16 kB L1 D Cache & 64 kB L2 Cache, and cache thrashed after encoding each frame.
- MCPS numbers on the hardware will vary with the I-Cache and D-Cache size and with the memory configuration/placement
- Program memory doesn't include the code size of the test bench and standard library functions
- Data memory should be aligned to desired byte-boundary to meet the performance/functionality requirement

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