Ittiam WMA LSL Decoder

WMA Lossless Decoder

Microsoft® Windows Media™ Audio Lossless (WMA LSL) is a lossless audio compression format, supporting upto 8 channels of audio data at sampling frequencies upto 192kHz.

Ittiam's WMA Decoder is an implementation of the WMA Lossless 9.0 Decoder (Windows Media Porting Kit (WMPK) and is provided subject to the terms and conditions of the Microsoft Corporation Implementation License Agreement to other Licensees of the same.

Features

- Decoding of WMA Lossless 9.0 Standard bitstream.
- Supports N2 profile - sample rates upto 96 kHz and upto 6 channels.
- Supports both 16 bit and 24 bit output.
- Implementation is fully compliant to the Windows Media Technology implementation test specification.
- Supports a simple C callable with flexible memory allocation scheme.
- Multi-channel, Reentrant software.
- The implementation has been tested on a variety of bitstreams and audio files for robustness and quality.
- Optimized for low footprint and processing power.

Decoder Validation

The WMA Lossless decoder implementation has been tested for conformance against the WMA LSL Test specification. The decoder has also been tested for robustness against bitstream errors.

Resource requirements on TI C64xPlus Processor

Function	MCPS	Pgm	Tables	Static	Scratch
	Peak	ROM (kb)		RAM (kb)	
Decode (N1 Profile)	30.26	58.1	0	43	3
Decode (N2 Profile)	143.78	58.1	0	168	3

Note N1 profile - 2 channel, 48kHz

N2 Profile - 6 channel, 96kHz

Note The Data Memory mentioned in the above Table does not include Input/ Output buffers.

Note MIPS for MCPS measurement on 0 wait-state memory access

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Details of Resource Requirement on C64xPlus

CPU Loading

CPU	Simulator		Hardware	
Description	Ave MCPS	Peak MCPS	Ave MCPS	Peak MCPS
N1 Profile (2 channel, 48kHz)	29.6	30.26	58.62	66.09
N2 Profile (6 channel, 96kHz)	133.97	143.78	252.16	311.64

Memory Usage

Profile	Program	Tables	Static	Scratch	Input	Output
N1 profile	58.1	0	43	3	0.1	12
N2 profile	58.1	0	168	3	0.1	72

Note:

- Memory numbers are in KB (Kilobytes)
- Performance numbers on Simulator generated with C64xPlus Cycle Accurate Simulator with 0 wait state memory access.
- Hardware configuration performance generated on a TMS320DM6446 processor with all the program and data placed in external memory, with cache configuration of 32KB L1 P Cache, 16 KB L1 D cache and 64 KB L2 cache, and cache thrashed after decoding each frame.
- MCPS numbers on the hardware will vary with the I-Cache and D-Cache size and with the memory configuration/placement.
- Program memory does not include the code size of the testbench and standard library functions.
- Data memory should be aligned to desired byte boundary to meet the performance/ functionality.