

# How to combine FPGAs and DSPs to get the best base station performance

With higher bandwidth requirements and OFDMA coming soon, intelligent partitioning between DSPs and FPGAs will deliver the best combination of features and cost-effectiveness.

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Suppliers of DSP chips and programmable logic may differ over which device type is best for new wireless system designs but the design strategies their customers are actually implementing is what's most important.

And today, designers are mixing PLDs and DSPs. "Intelligent partitioning" between these two device types gives wireless systems the best combination of features and cost-effectiveness.

Besides the obvious goals of meeting specifications, the practice of mixing DSPs and FPGAs brings a measure of future proofing as well as potential for risk-free cost reduction. This article expands on these design strategies and provides examples of FPGA+DSP system partitioning for wireless basestations that illustrate why combining programmable logic with DSP can assist designers with their projects.

## **Growing bandwidth requirements**

Market needs for higher data rates are driving the evolution of wireless cellular systems from narrowband 2G GSM, IS-95 systems to current-generation W-CDMA-based 3G and 3.5G systems supporting peak data rates up to 10 Mbps.

For future 3GPP long-term evolution specifications, complex signal processing techniques such as multiple-input multiple-output (MIMO) along with new radio technologies like orthogonal frequency-division multiple access (OFDMA) and multicarrier Code Division Multiple Access (MC-CDMA) are considered key to achieving target throughputs in excess of 100 Mbps.

Alternate OFDM-based broadband wireless systems such as WiMAX have similarly evolved, achieving transmission speeds in excess of 70 Mbps. The improvement in data rates has been possible primarily through the use of higher order modulation techniques and variable rate channel coding.

Complex spatial signal processing schemes such as beamforming and MIMO antenna techniques are also proven technologies for increasing data rates at the expense of additional hardware. These enabling technologies pose significant challenges for OEMs needing to design basestations that are not only scalable and cost-effective but also flexible and re-usable across multiple evolving standards.

## Basestation design requirements

Wireless systems designers need to meet a number of critical requirements including processing speed, flexibility, and time-to-market. These stringent requirements ultimately drive the hardware platform choice. Some of the major challenges include:

- **Processing bandwidth:** WiMAX broadband wireless systems have significantly higher throughput and data rate requirements than W-CDMA and cdma2000 cellular systems. To support these high data rates, the underlying hardware platform must have significant processing bandwidth. Additionally, several advanced signal processing techniques such as Turbo coding/decoding and front-end functions including fast Fourier transform/inverse fast Fourier transform (FFT/IFFT), beamforming, MIMO, crest factor reduction (CFR), and digital predistortion (DPD) are computationally intensive and require several billion multiply and accumulate (MAC) operations per second.
- **Flexibility:** WiMAX is a relatively new market and is currently in the initial development and deployment stages. Similarly 3GPP LTE is being defined and will go through numerous revisions before being finalized. It is still unclear which of the many "mobile broadband technologies" (i.e. WiMAX, Wibrow, Super 3G, LTE, Ultra 3G, etc.) will be embraced by the marketplace. Under this current scenario, having flexibility and re-programmability in the end product is necessary to provide a standards-agnostic or multi-protocol basestation. Systems offering this flexibility can significantly reduce the CAPEX and OPEX costs for wireless infrastructure OEMs and operators while alleviating risks posed by constantly evolving standards.
- **Cost-reduction path:** A valuable lesson learned from designing and deploying 3G systems is the importance of establishing a long-term cost-reduction strategy in the beginning. Evolving WiMAX and LTE standards are expected to stabilize. This will likely lead to a situation where cost of the final product will be more important than flexibility for OEMs and service providers to remain competitive in the marketplace. Choosing the right hardware platform for prototyping that provides a seamless cost-reduction path for production volumes will save millions of dollars in engineering costs that would otherwise be required for system re-design.

## System architecture design and logic task partitioning

Signal-processing data path and control operations make up the bulk of the processing load in a wireless basestation. Most architectures implement the system control, configuration, and the signal-processing data path using a combination of microcontrollers (MCUs), FPGAs and programmable DSPs.

The MCU controls the system, while the FPGA and DSP handle the data-flow processing. Systems with light processing demands and control-oriented tasks are implemented in software on a DSP; heavier loads are best implemented in FPGAs that provide significant parallel processing benefits. The combination of DSPs and FPGAs ensures complete system flexibility and offers reprogrammability to fix bugs or even support entirely different standards.

**The exact partitioning between FPGAs and DSPs depends on processing requirements; system bandwidth as well as system configuration; and the number of transmit and receive antennas. Figure 1 shows a typical DSP/FPGA partitioning for baseband physical layer (PHY) functions in an OFDMA-based system such as WiMAX or LTE.**

[Click here for Figure 1](#)

*Figure 1: DSP/FPGA partitioning for OFDMA systems.*

By incorporating advanced multiple antenna technologies, the throughput offered by such systems is expected to be between 75-100Mps. The baseband PHY functionality can be broadly categorized

into bit-level processing and symbol-level processing functions. Following is an overview of these functions and how FPGAs are used to complement DSPs for implementing both bit-level and symbol-level functions.

### **Bit-level processing**

The bit-level blocks include randomization, forward error correction (FEC), interleaving, and mapping to quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM) functions on the transmit side. The corresponding receive processing bit-level blocks are symbol de-mapping, de-interleaving, FEC decoding, and de-randomization. All bit-level functions except FEC decoding are relatively straightforward and not computationally intensive.

For example, randomization involves modulo-2 addition of the data bits with the output of a simple pseudo-random binary sequence generator. Although FPGAs offer more flexibility for bit-level manipulations than DSPs with fixed bus widths, the low computational complexity allows such functions to be easily implemented on DSPs.

Conversely, FEC decoding—including Viterbi decoding, Turbo convolutional decoding, Turbo product decoding, and LDPC decoding—are computationally intensive and consume significant bandwidth when implemented on DSPs. FPGAs are widely used to offload these functions and free up bandwidth on DSPs to perform other functions.

The same FPGA can also be used to interface to the MAC layer as well as implement certain lower MAC functions such as encryption/decryption and authentication. Altera's low-cost Cyclone II FPGAs are well suited to implement such DSP co-processing functionality.

### **Symbol-level processing**

Symbol-level functions in OFDMA systems include sub-channelization and de-subchannelization, channel estimation, equalization and cyclic prefix insertion, and removal functions. The time-to-frequency domain conversion and vice-versa are implemented using FFT and IFFT, respectively.

Channel estimation and equalization can be performed offline and involve more control-oriented algorithms that are better suited for DSPs. Conversely, FFT and IFFT functions are regular data path functions involving complex multiplications at very high speeds and are better suited for implementation on FPGAs.

Figure 2 shows the embedded DSP blocks contained in a high-end FPGA (Altera Stratix II device). DSP processors typically have up to eight dedicated multipliers, whereas Stratix II devices offer up to 384 18x18 dedicated multipliers providing throughputs of up to 346 GMACs, an order of magnitude higher than currently available DSPs.

[Click here for Figure 2](#)

**Figure 2:** *Embedded DSP blocks architecture in Stratix II FPGAs.* Such a massive difference in signal processing capability between FPGAs and DSPs is further accentuated when dealing with basestations employing advanced, multiple antenna techniques such as space time coding (STC), beamforming, and MIMO schemes.

The combination of OFDM-MIMO is widely regarded as a key enabler of higher data rates in current and future WiMAX and LTE wireless systems. Figure 1 shows multiple transmit and receive antennas employed at a basestation. In this station, symbol processing functions are implemented separately for each antenna stream before MIMO decoding is performed, producing a single bit-level data stream.

The symbol-level complexity grows linearly when the antennas implemented on DSPs perform operations in a serial manner. For example, when two transmit and two receive antennas are used,

the FFT and IFFT functions consume approximately 60 percent of a 1GHz DSP when the transform size is assumed to be 2048 points.

In contrast, a multiple antenna-based implementation scales very efficiently when implemented with FPGAs. FPGAs provide parallel processing and time-multiplexing between the data from multiple antennas. The same 2x2 antenna FFT/IFFT configuration can be implemented using less than five percent of a Stratix II 2S180 FPGA.

Multiple antenna schemes provide various benefits including higher data rates, array gain, diversity gain, and co-channel interference suppression. Beamforming and spatial multiplexing MIMO techniques are also computationally intensive, involving matrix decompositions and multiplications.

Specifically, Cholesky decomposition, QR decomposition, and singular value decomposition functions are useful in solving the linear set of equations common in these systems. While these functions quickly exhaust DSP capabilities, they are well suited for FPGAs using well known systolic array architectures that provide a more cost-effective solution by exploiting FPGA parallelism.

### **Digital IF processing**

Figure 3 shows data from a baseband channel card being sent to a RF card for subsequent digital intermediate frequency (IF) processing, including digital upconversion (DUC), crest factor reduction (CFR), and digital predistortion (DPD). Digital IF extends the scope of digital signal processing beyond the baseband domain to the antenna—to the RF domain.

This increases the flexibility of the system while reducing manufacturing costs. Moreover, digital frequency conversion provides greater flexibility and higher performance (in terms of attenuation and selectivity) than traditional analog techniques.

CFR and DPD functions are required to improve the efficiency of power amplifiers used in basestations. These functions also help to significantly reduce the cost of the overall RF card. Both CFR and DPD involve complex multiplications at sample rates as high as 100+Msps.

Similar to DUC, digital downconversion (DDC) is required on the receive side to bring the IF frequency down to baseband. Both DUC and DDC use complex filter architectures including finite impulse response (FIR) and cascaded integrator-comb (CIC) filters.

Advanced FPGAs provide hundreds of 18x18 multipliers running at speeds as high as 350-MHz. Not only does this provide a platform capable of processing multiple channels in parallel, it also yields a cost-effective, integrated single-chip solution.

[Click here for Figure 3](#)

*Figure 3: Digital IF Processing Functions.*

### **Conclusion**

As standards stabilize, the initial need for flexibility in basestations should subside. At this stage, high performance and a long-term cost-reduction path become critical for market success. ASIC implementation has typically been the chosen cost-reduction route.

Choosing FPGAs that have a risk-free migration path to low-cost structured ASIC technology will enable significant cost savings during the later stages of a product lifecycle. As an example Altera's HardCopy II technology provides a seamless, risk free migration path from Stratix II FPGAs to significantly lower cost HardCopy II Structured ASICs, while also increasing system performance and decreasing power consumption.

Concurrent application of DSPs and PLDs in wireless basestation designs will continue as an effective design approach. What's essential to product success is intelligent partitioning of basestation architecture derived from system throughput requirements and long-term cost considerations. This will ensure final products that are not only scalable and cost-effective, but flexible and reconfigurable across multiple evolving standards.

**About the author**

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