



## DSP

The heart of the D.Module.VC33 is the floating point digital signal processor TMS320VC33 from Texas Instruments, an enhanced version of the popular C31 processor. This DSP offers 32/40 bit floating point and 24/32 bit integer arithmetic with a maximum performance of 75 MIPS, 150MFLOPS, 34K x 32 Bits Words internal dual access memory, instruction cache, a synchronous serial port, two timers and DMA controller.

The serial port provides a direct connection to industry standard Codecs, A/D and D/A converters. High Speed data transfer up to 37.5 MBit / sec is possible. This also provides an efficient data path for multiprocessor coupling. Data transfer between the serial port and internal and external memory is possible under DMA control.

## MEMORY

The DSP itself is equipped with 34k x 32 Bit words internal dual access memory. The 64K x 32 Bits (256 kByte) static SRAM operates with one wait state, providing a transfer rate of 37.5 MWords per second (150 MByte/sec.). Optionally, a 1 MByte memory configuration (256KWords x 32 Bit) is available.

512 kByte Flash Memory are integrated for non-volatile data and program storage, organised as 512k x 8 bit. The Flash Memory is divided in multiple sectors of 64 kByte. Each sector can be erased independently and re-programmed on a Byte basis. The DSP has direct access to the Flash Memory: Identification, Sector-Erase and Programming is handled by BIOS functions which effectively encapsulate the programming algorithms. The onboard wait state logic generates the required wait states for Flash Memory accesses while retaining fast access to other on board devices.

For external interfaces and memory expansion two pre-decoded memory areas and select signals exist. The IOSEL memory range is primarily intended for the connection of parallel interface data acquisition and communication devices. The MEMSEL area provides access to a maximum of 4MWords external memory expansion. Both areas have individual wait state generation, 1 to 7 wait states and external ready are supported. The user-configurable CPLD can be used to implement supplementary logic functions, e.g. a SDRAM controller.

## CLOCKS

An on board crystal generates the DSP master clock. Alternatively, an external clock input is pro-

vided to synchronise the DSP module's operating frequency to an external clock master. Additional clocks for peripherals can be generated by the two 32 bit timers. The Serial Port features its own clock generation circuitry based on the DSP clock or external bit clocks.

## POWER SUPPLY

The D.Module.VC33 operates from a single 3.3 to 5.5V power supply. Secondary voltages for RS232 are generated on board by charge pumps. A micro-processor supervisor circuit controls the power supply and holds the board in reset if the supply voltage is below its limit. The power consumption is exceptionally low. In idle mode the module requires only 6 mA standby current, while still providing wake-up on interrupt and wake-up on UART reception functionality.

## EXTERNAL BUS INTERFACE

The external bus interface provides a 32 bit wide data bus, 24 address lines and control signals. Wait states are software configurable. For both external expansion memory areas, 1 to 7 wait states are individually configurable.

The external bus is fully 5V compliant and tolerant, independent of the module's power supply. Zero propagation delay FET switches are used to implement level shifting and isolate the data bus during on board accesses.

The user-configurable CPLD can be used to adapt the bus interface to different formats - e.g. to connect ISA bus devices - by integrating the required state-machines and decoders. Glueless integration into a variety of systems is made possible.

## UART

The D.Module.VC33 UART features 32 Byte transmit and receive FIFOs and automatic flow control for RTS/CTS and Xon/Xoff handshake. This allows DMA driven data transfers without any CPU core involvement.. The UART is fully supported by the D.Module.BIOS: initialisation and communication functions are provided. Standard baud rates up to 460 kBaud and 5.8 bit data formats are supported.

## USER-CONFIGURABLE CPLD

One of the major challenges in DSP design is the integration into a host system and interfacing peripherals. To facilitate this we have integrated a 64 macrocell in-system programmable CPLD. 16 bit data

bus, address lines, control and clock signals are pre-connected to the DSP. The CPLD can be re-programmed via the module's Set-Up Utility program by uploading the programming file or via a download cable connected to the printer port of a PC.

Additional I/O ports, interrupt controller, host interface, SPI or I<sup>2</sup>C serial interface, bus interface adaptation and clock generation are some of the possible applications. 32 I/Os are available and can be configured as input, output 3State or bi-directional signals.

## BOOT OPTIONS

By default, the D.Module.VC33 is boot loaded from the Flash Memory. In this mode, the BIOS and the Configuration Utility are loaded first. The nSETUP signal (IN0) is sampled, if low, Set-Up mode is entered which allows to store programs and data in the Flash Memory, programming the CPLD and executing diagnostic functions via a RS232 terminal connection. If nSETUP is not asserted, the BIOS boot-loader loads the application program and executes it.

The BIOS provides a bootload function which allows the application program to be bootloaded from any arbitrary memory mapped device, e.g. a host micro processor, or via the synchronous serial interface.

## MODULE CONFIGURATION

A module configuration register provides full software control for operation mode, watchdog, reset and power down signals, interrupt configuration and wait state generation.

The D.Module.VC33 provides a unique Module Configuration File which is permanently stored in the Flash Memory. The Configuration File is similar to the \*.ini Files used by Microsoft Windows® and allows to store human-readable ASCII data for configuration such as communication parameters, signal-processing coefficients, temperature compensation tables etc. Thus maintenance and modifications of installed installations is greatly simplified: Edit the configuration file and upload the modified version in Set-Up mode.

## RESET and WATCHDOG

A micro-processor supervisor circuit monitors the power supply and resets the module during power-up, power-down and brown-out conditions. A re-triggerable single-shot guarantees a minimum reset pulse width of 140 msec.

A debounced external reset input can be used to connect a system reset signal or a push-button for manual reset. A reset output is controlled via the module configuration register and can be used to initialise external peripherals.

A watchdog provides security against program lock-ups and hardware failures as required by most embedded applications. The watchdog timer must be re-triggered at least every 1.6 seconds, otherwise a reset is generated. The watchdog trigger is generated by the module configuration register.

## EXTERNAL INTERRUPTS

The D.Module.VC33 provides four external, falling edge triggered, interrupt inputs. These interrupts are multiplexed with internal interrupt sources (UART and User-CPLD) via the Module Configuration Register. Interrupts can also be used to trigger a DMA event.

## BIOS

The D.Module.BIOS is an application programming interface for all on board resources. It encapsulates the hardware dependencies and provides functions for

- Module initialisation
- UART initialisation , send and receive functions
- Flash Memory programming support: identify device, erase a sector, program
- Module configuration: set and clear bits and bit-fields in the module configuration register
- Miscellaneous functions: install interrupt handler, access to the DSP's registers from a C environment, bootload and delay.

These functions are identical on all D.Modules and help to maintain program portability throughout the D.Module family. The BIOS is written in hand-coded Assembler language to achieve optimum performance. All functions are C and Assembler callable. The BIOS occupies only 1k x 32 words memory.

## MEMORY MAP

The module can be used in two modes: MP-Mode supports a direct interrupt vectoring scheme but does not allow boot-mode. MCBL-Mode is the default configuration of the D.Module.VC33, in which the boot loader is enabled. In this mode the interrupt vector table is located in internal RAM.

## MEMORY MAP (MCBL Mode, default after Reset)

Address	Memory	Wait States	Comment
0x000000 .. 0x000FFF	ROM	-	internal Boot Loader ROM
0x001000 .. 0x0013FF	SRAM	auto (1)	BIOS
0x001000 .. 0x010FFF .. 0x040FFF			64K x 32 256K x 32
0x400000 .. 0x4FFFFFF			FLASH
0x500000 .. 0x500007	UART	auto	UART, connected to D0..D7
0x600000 .. 0x600003	Configuration Registers	auto	Configuration Registers
0x700000 .. 0x7000FF 0x700100 .. 0x7FFFFFF	CPLD	auto	User configurable CPLD Aliases of CPLD
0x800000 .. 0x803FFF	int. RAM2	-	internal RAM Block 2
0x804000 .. 0x807FFF	int. RAM3	-	internal RAM Block 3
0x808000 .. 0x8097FF	int. Peripherals	-	DSP internal Peripherals (Timer, Ser. Port, etc)
0x809800 .. 0x809BFF	int. RAM0	-	internal RAM Block 0 (Note: 0x809800, 0x809801 are used as stack during bootload)
0x809C00 .. 0x809FC0	int. RAM1	-	internal RAM Block 1
0x809FC1 .. 0x809FFF	int. RAM1	-	internal RAM Block 1, Interrupt Vector Table
0x80A000 .. 0xBFFFFFF	nIOSEL	1..7 or external	nIOSEL active
0xC00000 .. 0xFFFFFFFF	nMEMSEL	1..7 or external	nMEMSEL active

## MEMORY MAP (MP Mode)

Address	Memory	Wait States	Comment
0x000000 .. 0x00003F	SRAM	auto (1)	Interrupt Vector Table
0x000040 .. 0x000FFF			
0x001000 .. 0x0013FF			BIOS
0x001400 .. 0x00FFFF .. 0x03FFFF			64K x 32 256K x 32
0x400000 .. 0x4FFFFFF	FLASH	auto	Flash Memory, 8 bit wide, connected to D0..D7
0x500000 .. 0x500007	UART	auto	UART, connected to D0..D7
0x600000 .. 0x600003	Configuration Registers	auto	Configuration Registers
0x700000 .. 0x7000FF	CPLD	auto	User configurable CPLD
0x800000 .. 0x803FFF	int. RAM2	-	internal RAM Block 2
0x804000 .. 0x807FFF	int. RAM3	-	internal RAM Block 3
0x808000 .. 0x8097FF	int. Peripherals	-	DSP internal Peripherals (Timer, Ser. Port, etc)
0x809800 .. 0x809BFF	int. RAM0	-	internal RAM Block 0
0x809C00 .. 0x809FFF	int. RAM1	-	internal RAM Block 1
0x80A000 .. 0xBFFFFFF	nIOSEL	1..7 or external	nIOSEL active
0xC00000 .. 0xFFFFFFFF	nMEMSEL	1..7 or external	nMEMSEL active

## BOARD CONFIGURATION REGISTERS

### CFG\_MODE (Address 0x600000)

Bit	D31..D5	D4	D3	D2	D2	D0
<b>Signal</b>	undefined	reserved	Reset Source (read only)	Watchdog Trigger	MCBL / nMP	INTMUX
<b>Bit = 0:</b>	-	-	Power-On or manual Reset	watchdog trigger remains unchanged	MP mode	DSP interrupt inputs = Boot Config
<b>Bit = 1:</b>	-	-	Reset caused by Watchdog Timeout	toggles watchdog trigger each time a '1' is written to this bit	MCBL mode	DSP interrupt inputs = external interrupts
<b>Reset State</b>	X	0	?	0	1	0

### CFG\_INT (Address 0x600001)

Bit	D31..D5	D4, D3	D2, D1	D0
<b>Signal</b>	undefined	INT3 MUX	INT2 MUX	INT1 MUX
		00 - ext. Interrupt nINT3 01 - CPLD Interrupt 10 - UART Interrupt 11 - UART TX DMA Request	00 - ext. Interrupt nINT2 01 - CPLD Interrupt 10 - UART Interrupt 11 - UART RX DMA Request	0 - ext. Interrupt nINT1 1 - CPLD Interrupt
<b>Reset State</b>	X	00	00	0

### CFG\_WAIT (Address 0x600002)

Bit	D31..D6	D5 .. D3	D2 .. D0
<b>Signal</b>	undefined	nMEMSEL Wait States	nIOSEL Wait States
		000 - external (nWAIT) 001 - 1 Wait States ... 111 - 7 Wait States	000 - external (nWAIT) 001 - 1 Wait States ... 111 - 7 Wait States
<b>Reset State</b>	X	00	0

### CFG\_RES (Address 0x600003)

Bit	D31..D6	D5, D4	D3	D2	D1	D0
<b>Signal</b>	undefined	reserved	UART_RESET	CPLD_RESET	nRESOUT	RS232_nSHDN
<b>Bit = 0:</b>	-	-	UART active	CPLD in Reset	nRESOUT low	RS232 line transmitter off
<b>Bit = 1:</b>	-	-	UART in Reset	CPLD active	nRESOUT high impedance	RS232 line transmitter on
<b>Reset State</b>	X	0	1	0	0	0

## SIGNAL DESCRIPTION

### EXTERNAL BUS INTERFACE (all signals 5V TTL compatible and tolerant)

Signal	Pin	Type	Description
A0 .. A23	U9 .. U14, V2 .. V14, A14..A18	O	address bus
D0 .. D31	V15 .. V30 U15.. U30	I/O/Z	data bus, three-state (Z) if on board components are accessed, only active on access to nIOSEL and nMEMSEL address range
nRD	U2	O	active low read select signal (data to DSP)
nWR	U5	O	active low write select signal (data from DSP)
nIOSEL	U8	O	active low memory select signal
nMEMSEL	V31	O	active low memory select signal
BUSCLK	U6	O	DSP H1clock, all bus cycles are synchronous to this clock, use BUSCLK to latch the state of the external bus
nSTRB	B21	O	active low strobe output from DSP (provided for D.Module.C31eco compatibility only)

### SERIAL PORT (all signals 5V TTL compatible and tolerant)

Signal	Pin	Type	Description
DAT_RX0	A26	I/O	receiver serial data input or general purpose I/O
CLK_RX0	A27	I/O	receiver serial clock input or output or general purpose I/O
FS_RX0	A28	I/O	receiver frame sync input or output or general purpose I/O
DAT_TX0	A29	I/O	transmitter serial data output or general purpose I/O
CLK_TX0	A30	I/O	transmitter serial clock input or output or general purpose I/O
FS_TX0	A31	I/O	transmitter frame sync input or output or general purpose I/O

### TIMERS, FLAGS (all signals 5V TTL compatible and tolerant)

Signal	Pin	Type	Description
TIMER0	A21	I/O	Timer 0 input or output or general purpose I/O
TIMER1	A22	I/O	Timer 1 input or output or general purpose I/O
FLAG0	A23	I/O	DSP XF0 Flag, input or output
FLAG1	A24	I/O	DSP XF1 Flag, input or output

### CLOCK

Signal	Pin	Type	Description
DSPCLK	A7	I	external clock input at 1x DSP frequency if jumper JPCLK is closed <b>not 5V tolerant</b>

## EXTERNAL INTERRUPTS (all signals 5V TTL compatible and tolerant)

Signal	Pin	Type	Description
nINT0	U3	I	external interrupt inputs, falling edge triggered, internal pull-up resistor
nINT1	U4	I	
nINT2	A19	I	
nINT3	A20	I	
nIACK	B22	O	DSP IACK signal, can be used by the IACK instruction to acknowledge interrupt processing to external hardware

## USER-CONFIGURABLE CPLD (all signals 5V TTL compatible and tolerant)

Signal	Pin	Type	Description
PRG_IO0 ..	B2 ..	I/O	programmable I/O, can be used for any purpose, function depends on the PLD-program, configurable as input, output, 3State or bi-directional
PRG_IO15	B17	I/O	
PRG_IO16 ..	T2 ..	I/O	
PRG_IO31	T17	I/O	
USER_TMS	B28	I	JTAG programming signals for User-Configurable CPLD
USER_TCK	B29	I	these signals are provided for ATE equipment only, normally, the CPLD is (re-)programmed via a terminal program in Setup-Mode
USER_TDI	B30	I	
USER_TDO	B31	O	

## RESET (all signals 5V TTL compatible and tolerant)

Signal	Pin	Type	Description
nRESIN	A9	I	debounced reset input, active low, on board pull-up resistor
nRESOUT	U7	O	reset output, active low, asserted while module is in reset, controlled via module configuration register

## UART, RS232/422

Signal	Pin	Type	Description
RTS / nTxD	A2	O	RS232 Request to Send handshake signal RS422 inverting transmitter output
TxD	A3	O	RS232 transmitter output RS422 non-inverting transmitter output
CTS / nRxD	A4	I	RS232 Clear to Send handshake signal RS422 inverting receiver input
RxD	A5	I	RS232 receiver input RS422 non -inverting receiver input
IN0 (nSETUP)	A11	I	general purpose input, on board pull-up resistor, sampled at reset to determine Setup-Mode <b>(not 5V tolerant !)</b>
IN1	A12	I	general purpose input, on board pull-up resistor <b>(not 5V tolerant !)</b>

## POWER SUPPLY

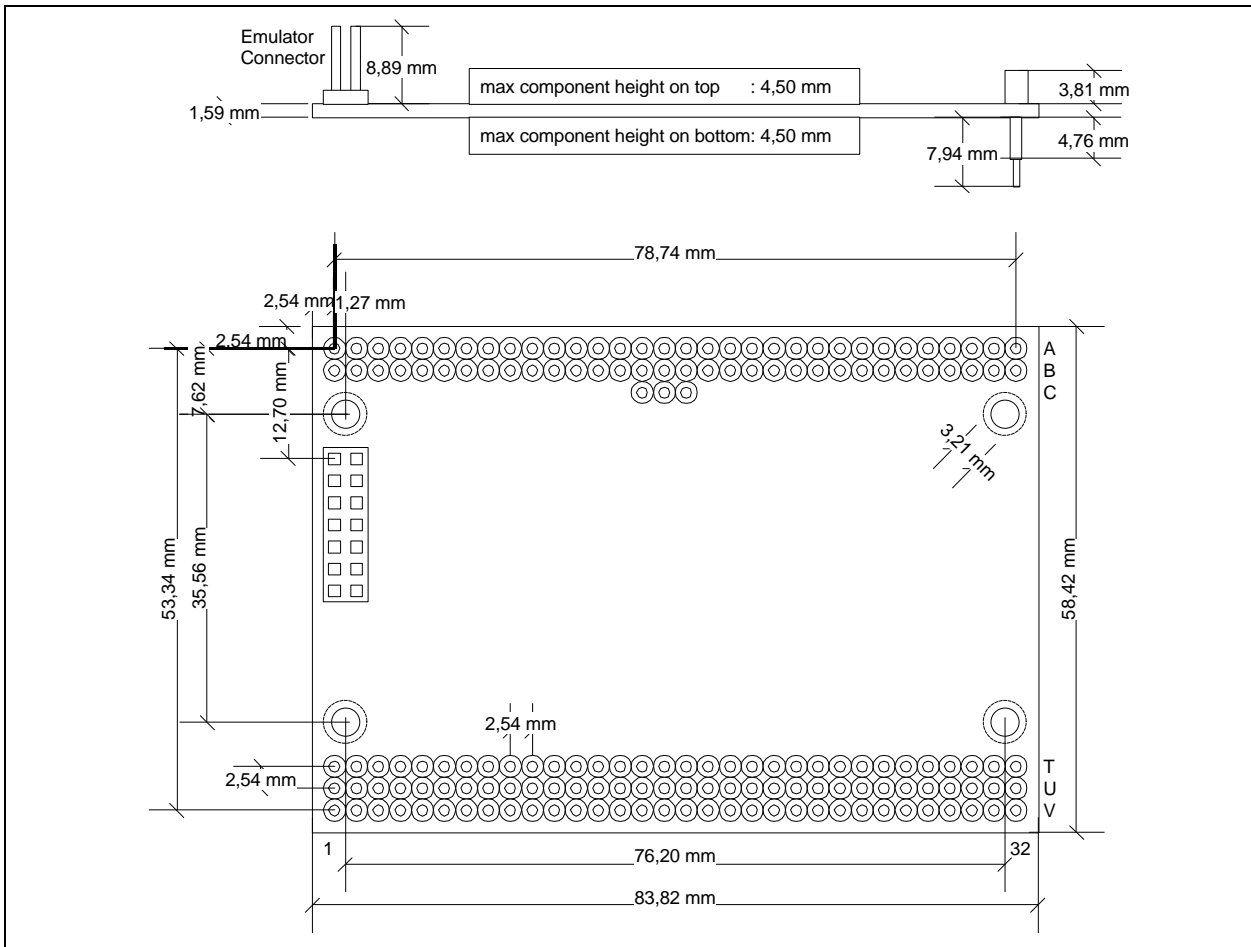
Signal	Pin	Type	Description
VCC	A1, B32	P	power supply, use either A1/B1 or A32/B32 pin pair to avoid loops
GND	A32, B1	P	power supply, use either A1/B1 or A32/B32 pin pair to avoid loops
+AVCC	C17, U1	P	additional supply pins to route a positive analogue power supply line to a daughter module stacked on top of the DSP module, not connected
-AVCC	C15, U31	P	additional supply pins to route a negative analogue power supply line to a daughter module stacked on top of the DSP module, not connected
AGND	C16, U32	P	additional supply pins to route a 0V analogue power supply line to a daughter module stacked on top of the DSP module, not connected

## PINOUT

Pin	A	B	C	T	U	V
1	VCC	GND		VCC5 * <sup>1</sup> (nc)	+AVCC * <sup>1</sup> (nc)	VCC5 * <sup>1</sup> (nc)
2	RTS / nTxD	PRG_IO0		PRG_IO16	nRD	A6
3	TxD	PRG_IO1		PRG_IO17	nINT0	A7
4	CTS / nRxD	PRG_IO2		PRG_IO18	nINT1	A8
5	RxD	PRG_IO3		PRG_IO19	nWR	A9
6	GND	PRG_IO4		PRG_IO20	BUSCLK	A10
7	DSPCLK	PRG_IO5		PRG_IO21	nRESOUT	A11
8	GND	PRG_IO6		PRG_IO22	nIOSEL	A12
9	nRESIN	PRG_IO7		PRG_IO23	A0	A13
10	nWAIT	PRG_IO8		PRG_IO24	A1	A14
11	IN0 (nSETUP)	PRG_IO9		PRG_IO25	A2	A15
12	IN1	PRG_IO10		PRG_IO26	A3	A16
13	GND	PRG_IO11		PRG_IO27	A4	A17
14	A19	PRG_IO12		PRG_IO28	A5	A18
15	A20	PRG_IO13	-AVCC (nc)	PRG_IO29	D16	D0
16	A21	PRG_IO14	AGND (nc)	PRG_IO30	D17	D1
17	A22	PRG_IO15	+AVCC (nc)	PRG_IO31	D18	D2
18	A23	PRG_IO16		nc	D19	D3
19	nINT2	nc		nc	D20	D4
20	nINT3	nc		nc	D21	D5
21	TIMER0	nSTRB		nc	D22	D6
22	TIMER1	nIACK		nc	D23	D7
23	FLAG0	nc		nc	D24	D8
24	FLAG1	nc		nc	D25	D9
25	nc, reserved	nc		nc	D26	D10
26	DAT_RX0	nc		nc	D27	D11
27	CLK_RX0	GND		nc	D28	D12
28	FS_RX0	USER_TMS		nc	D29	D13
29	DAT_TX0	USER_TCK		nc	D30	D14
30	CLK_TX0	USER_TDI		nc	D31	D15
31	FS_TX0	USER_TDO		nc	-AVCC * <sup>1</sup> (nc)	nMEMSEL
32	GND	VCC		GND * <sup>1</sup>	AGND * <sup>1</sup> (nc)	GND * <sup>1</sup>

Signals marked with \*1) are provided for compatibility to the miniKit family of DSP boards only, do not use for new designs!

## MECHANICAL DIMENSIONS



D.Module.VC33

## ELECTRICAL CHARACTERISTICS

### OPERATING CONDITIONS, DC PARAMETERS

Supply Voltage VCC	3.3 - 5.5V
Power Consumption	idle: 6 mA, typical: 100 mA
Operating Temperature	0..+70°C
High Level Input Voltage	min. 2V, max. 5.5V (3.5V on inputs not 5V tolerant)
Low Level Input Voltage	min. -0.2V, max. 0.8V

Power Consumption largely depends on the selected clock frequency and the application. The idle power consumption is measured while the module is held in reset, the maximum value is calculated based on Texas Instruments datasheet information and experimental results.

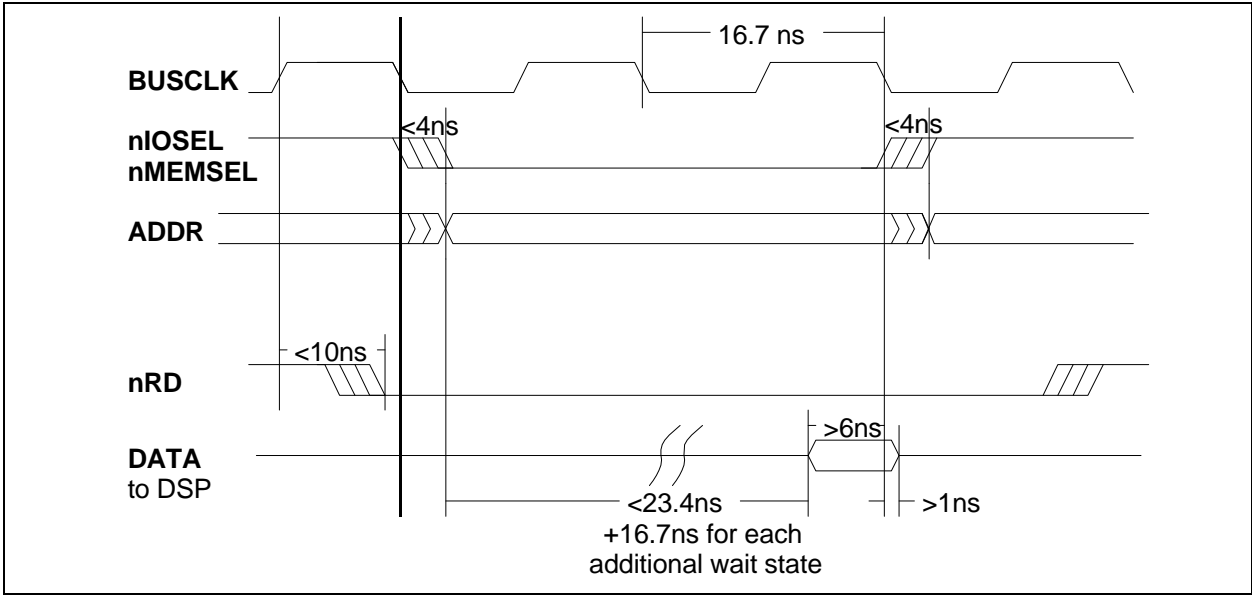
## TIMINGS

The external bus timings are shown in the following diagrams. Timings are based on 120 MHz DSP clock and assume a max. capacitive load of 80pF total. If the external capacitive load on Address and Control Signals should exceed 40pF please buffer

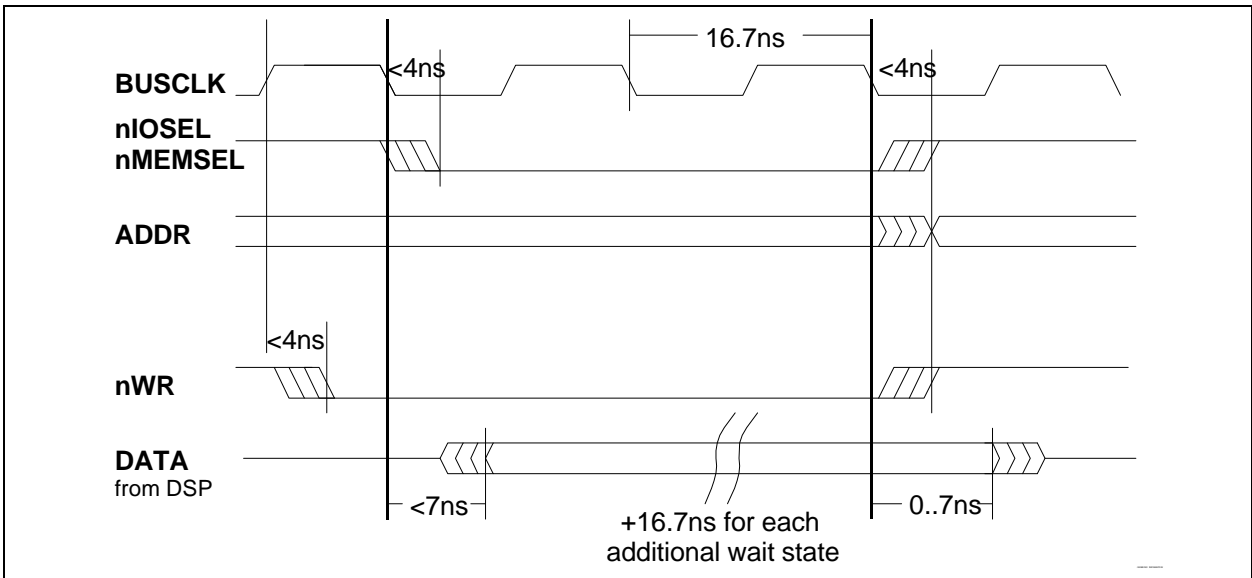
these signals. For Serial Port timings please refer to the Texas Instruments TMS320VC33 datasheet SPRS087.

## EXTERNAL BUS TIMINGS

### READ



### WRITE



D.Module.VC33

## ORDERING INFORMATION

D.Module.VC33-120-S0	TMS320VC33 DSP Computer Module 120 MHz operation, 256 kByte SRAM, 512 kByte Flash Memory
D.Module.VC33-150-S0	TMS320VC33 DSP Computer Module 150 MHz operation, 256 kByte SRAM, 512 kByte Flash Memory
D.Module.VC33-120-S2	TMS320VC33 DSP Computer Module 120 MHz operation, 1 MByte SRAM, 512 kByte Flash Memory
D.Module.VC33-150-S2	TMS320VC33 DSP Computer Module 150 MHz operation, 1 MByte SRAM, 512 kByte Flash Memory
Options: -422	RS422 line interface
DS.VC33	Board Development Support Base Package Support Software, BIOS license, CPLD library, CPLD programming adapter Base Board, User's Guide and BIOS Reference Manual
TMDS3240130	Texas Instruments Code Composer IDE including Code Generation Tools (Assembler, Linker, optimizing C-Compiler), Simulator and C Source Debugger with enhanced data visualization capabilities
XDS510pp_Plus-JTAG	Spectrum Digital portable JTAG Emulator, connected to PC printer port
XDS510-JTAG	Texas Instruments Emulator 16 bit ISA-bus card for PC and JTAG Emulator Head
701700	SPI525 Spectrum Digital Emulator, PCI bus card, variable voltage JTAG Head

### ADDITIONAL OPTIONS ON VOLUME PURCHASE

For volume purchase D.SignT offers customer-specific modifications of the hardware either to reduce costs through reduced functionality or to increase functionality to meet the customers application requirements. Extensive experience in custom designs and the powerful engineering tools of our development department bring your application and our DSP know how together for your solution. Please contact D.SignT directly.

### TECHNICAL SUPPORT

Our products include free of charge technical support. You can reach the technical support by e-mail (support@dsigt.de) phone or fax.

### PRICING

Please ask for our current price list and volume discounts.

### AVAILABILITY

Our standard D.Modules are available typically ex-stock. For special modifications or non-standard D.Modules please consult our sales department.

### WARRANTY

All D.Modules come with a warranty of 12 month.

D.Module.VC33

For additional information contact your local distributor who will also support you after your purchase or contact D.SignT directly.

**Distributed and supported locally by**

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