X5-RX

V0.1

Innovative Integration
... real time solutions!

PCI Express XMC Module with Four 200 MSPS 16-bit A/Ds, Virtex5 FPGA, 512MB DRAM/ 4MB SRAM

FEATURES

- Four 200 MSPS 16-bit A/D channels
- +/-1V, DC-Coupled, 50 ohm, SMA inputs
- Xilinx Virtex5, SX95T
- 512MByte DDR2 DRAM
- 4MByte QDR-II SRAM
- 8 RocketIO private links, 2.5 Gbps each
- >1 GB/s, 8-lane PCI Express Host Interface
- Power Management features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

APPLICATIONS

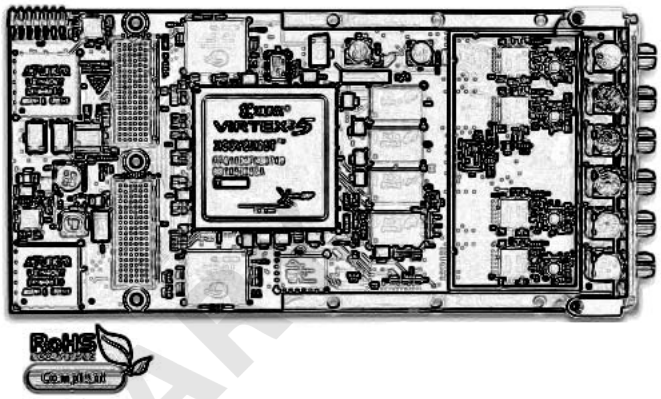
- Wireless Receivers
- RADAR
- Medical Imaging
- High Speed Data Recording
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ Host Tools

MATLAB

XILINX®



RoHS Compliant

DESCRIPTION

The X5-RX is a high performance digitizing and signal processing module for wireless, RADAR and medical imaging applications. The FPGA computing core supports real-time 200 MHz signal acquisition and processing for channelization, down-conversion and spectral analysis. For digitizing, the module features four simultaneously sampling 16-bit, 200 MSPS A/Ds.

A Xilinx Virtex5 SX95T with 512MB DDR2 DRAM and 4MB QDR-II memory provide a very high performance DSP core that is tightly integrated with the I/O and PCI Express interface. The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates exceeding 300 GMACs per second.

The X5 XMC modules couple Innovative's powerful Velocia architecture with a high performance, 8-lane PCI Express interface that provides over 1 GB/s sustained transfer rates to the host. Private links to host cards with > 1.6 GB/s capacity using P16 are provided for system integration.

The X5 family logic can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

IP libraries for the FPGA are also available for down-conversion and channelization of up to 4096 simultaneous channels, baseband demodulation for PSK, FSK and MSK, and spectral analysis. MATLAB simulation models are provided that support logic integration in to the X5-RX Framework Logic.

Software tools for host development include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features and use are provided.

03/01/09

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This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X5- RX (DC Coupled)	80222-0	PCI Express XMC module with four channels of 200 MSPS, 16-bit A/Ds, DC-coupled input, Virtex5 SX95T FPGA, 4MB SRAM, 512MB DRAM.
X5- RX (AC Coupled)	80222-1	PCI Express XMC module with four channels of 200 MSPS, 16-bit A/Ds, AC-coupled input, Virtex5 SX95T FPGA, 4MB SRAM, 512MB DRAM.
Logic and IP Cores		
X5-RX FrameWork Logic	55028	X5-RX FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
IP-PSK DEMOD	58001	PSK demodulator, N=2,4,8,pi/4
IP-FSK DEMOD	58002	FSK demodulator
IP-TINY DDS	58003	Tiny DDS, 1/3 size of Xilinx DDS with equal SFDR
IP-RI-MMDC16	58004	IP core for 16 independent DDC channels, netlist version, Virtex5 SX95 target
IP-RI-MMDC32	58005	IP core for 32 independent DDC channels, netlist version, Virtex5 SX95 target
IP-RI-CHTU128/256	58006	IP core for 128 or 256 independent DDC channels, netlist version, Virtex5 SX95 target
IP-RI-CHTU32/4096	58007	IP core for 32 to 4096 equi-spaced DDC channels, netlist version, Virtex5 SX95 target
Cables		
MMCX Hydra10	67068	IO cable with 10 terminations to coax cables with BNC (female), 1 meter
Adapters		
XMC-PCIe x1 Adapter	80172-0	PCI Express Carrier card for XMC PCI Express modules, x1 lanes
XMC- PCIe x8 Adapter	80173-0	PCI Express Carrier card for XMC PCI Express modules, x8 lanes
XMC-PCI Adapter	80167	PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-cPCI Adapter	80207	3U Compact PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
Embedded PC Host		
Embedded PC XMC host	90199	eInstrument embedded PC with Linux or Windows, USB, SATA, Gigabit Ethernet, dual HDD option, two XMC modules for standalone applications. Optional dual HDD for datalogging.
Low Power Embedded PC XMC host	90201	eInstrument embedded PC with Intel Atom, Linux or Windows, USB, SATA, Gigabit Ethernet, dual HDD option, two XMC modules for standalone applications. Optional dual HDD for datalogging.

X5-RX

Standard Features

Analog	
Inputs	4
Input Range	+/- 1V
Input Type	Single ended, DC coupled (-0) or AC coupled (-1)
Input Impedance	50 ohm
A/D Device	Texas Instruments ADS5485
A/D Resolution	16-bit
A/D Sample Rate	1 MHz to 200 MHz

FPGA	
Device	Xilinx Virtex5 XC5VSX95T-1FF1136C
Speed Grade	-1 (commercial)
Size	~9M gate equivalent
Flip-Flops	69120
Multipliers	640
Slice	17280
Block RAMs	296 (5328 Kbits)
Rocket IO	16 lanes @ 2.5 Gbps
Configuration	SelectMAP from on-board FLASH FLASH holds 2 images JTAG during development

Memories	
DRAM Size	512 MB total 4 devices @ 64Mx16 each
DRAM Type	DDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	3.8 GB/ sustained transfer rate
SRAM Size	4 MB total 2 devices @ 512Kx32 each
SRAM Controller	Two independent SRAM controllers implemented in FPGA logic
SRAM Type	QDR-II
SRAM Rate	1.2 GB/s sustained transfer rate for read and write simultaneously (2.4 GB/s total)

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Host Interface	
Type	PCI Express; 8 lanes
Sustained Data Rate	1 GB/s
Protocol	PCI Express with Velocia packet system
Connector	XMC P15
Interface Standard	PCIe 1.0a; VITA 42.3
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Sources	Onboard low jitter fixed oscillator, 160MHz default frequency
	External: Sine source 10 to 160 MHz, 0.3-3.3Vp-p (-6.47 to 14.3 dBm) AC-coupled, 50-ohm terminated
Jitter	Internal: 340 fs total
	External: 90 fs additive
Triggering	External or software; Continuous or N-sample-wide frame
Ext Trigger	MMCX female, LVTTL (0 to 3.3V max) DC-coupled, 50-ohm terminated.
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.

Acquisition Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

P16 Digital IO	
Rocket IO Channels	8
Rocket IO data rate	2.5 Gbps/lane (2 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	33
Signal Standard	LVTTL (3.3V)
Drive	+/-12 mA (programmable in logic)
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g
Hazardous Materials	Lead-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Supply Voltage, VPWR to GND	+4.5	+12.5	V	
Analog Input Voltage, Vin+ or Vin- to GND	-5.7	+5.7	V	
Operating Temperature	0	70	C	Non-condensing, forced air cooling required
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS					
Parameter	Min	Typ	Max	Units	Conditions
Supply Voltage	+3.15	+3.3	+3.45	V	
Supply Voltage	+11	+12	+13	V	
Operating Temperature	0		60	C	Non-condensing, forced air cooling required
Forced Air Cooling	2**	5	-	CFM	** All systems should be characterized to determine the cooling requirements.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
Analog Input Bandwidth	TBD	MHz	-3dB
SFDR	TBD	dB	
S/N	TBD	dB	
THD	TBD	%	
ENOB	TBD	bits	
Channel Crosstalk	TBD	dB	
Noise	TBD	mVp-p	
Noise Floor	TBD	dB	
Power Consumption	35	W	
Gain Error	<0.02	% of FS	Calibrated
Offset Error	<500	µV	Calibrated

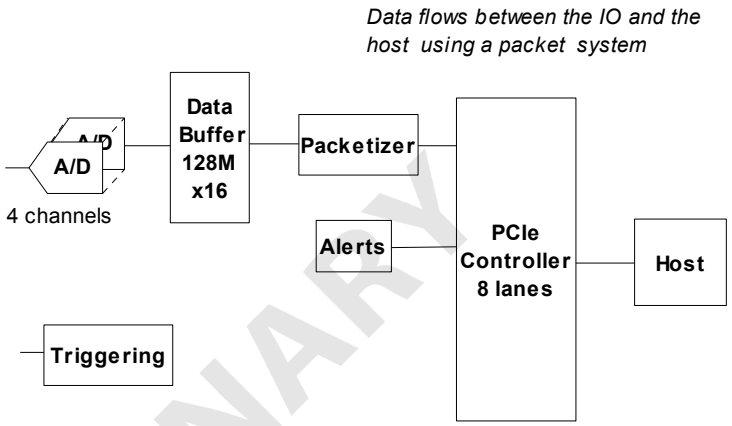
X5-RX

Architecture and Features

The X5-RX module architecture integrates analog IO with an FPGA computing core, memories and PCI Express host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates making it ideal as a front-end for demanding applications in wireless, RADAR and medical imaging applications.

Analog IO

The analog front end of the X5-RX module has four simultaneously sampling channels of 16-bit, 200 MSPS A/D input. The A/Ds are directly connected to the FPGA for minimum data latency. In the standard logic, the A/Ds have an interface component that receives the data, provides digital error correction, and a FIFO memory for buffering. The digital error correction is used to compensate for gain and offset errors. A non-volatile ROM on the card is used to store the calibration coefficients for the analog and is programmed during factory test.



X5 Architecture

The A/D channels operate synchronously for simultaneously sampling systems using the external clock input. Controls for triggering allow precise control over the collection of data and are integrated into the FPGA logic. Trigger modes include frames of programmable size, external and software. Multiple cards can sample simultaneously by using external trigger inputs. The trigger component in the logic can be customized in the logic to accommodate a variety of triggering requirements.

FPGA Core

The X5 Module family has a Virtex5 FPGA and memory at its core for DSP and control. The Virtex5 FPGA is capable of >300x10^9 MACs (SX95T operating at 500 MHz internally), about 20x faster than competing DSPs. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to 512MB of DDR2 DRAM capable of 3.8 GB/s data transfer rate and two independent banks of 2 MB QDR SRAM, each capable of 1.2GB/s transfer rate in each direction. These memories provide the FPGA working space for computations typically required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. A DRAM buffer control component in the FPGA implements a large virtual FIFO buffer in the DRAM that is used for system data buffering and algorithm support.

The X5 module family uses the Virtex5 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the dataflow, signal processing, controls and host interfaces, allowing complete customization of the X5 module functionality.

PCI Express Host Interface

The X5 architecture delivers over 1 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is

transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex5 FPGA using 8 Rocket IO ports, for a maximum bit rate of over 20 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 200 MB/s per lane. Since PCI Express is not a share bus, but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

Private Data Links

The X5 module family has private data links on the P16 connector that can be used for system integration. The P16 connector has 8 Rocket IO links, each capable of 2.5 Gbps, and 16 sideband signals. The 8 RIO lanes can be used to provide low-latency, high rate data to the system in addition to the PCI Express interface. Maximum data rates, with deterministic performance can be implemented in performance-driven systems using little or no protocol. For more complex systems, protocols such as Aurora can be used.

Module Management

The data acquisition process can be monitored using the X5 alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the X5 cards easier to integrate into larger systems.

FPGA Configuration

The X5 modules have a 128Mb FLASH that holds the FPGA application image. The FLASH can be reprogrammed in-system using a software applet for field upgrades.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx cables such as Platform USB and Parallel IV Cable.

Software Tools

Software development tools for the X5 modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every X5 module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the X5 performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

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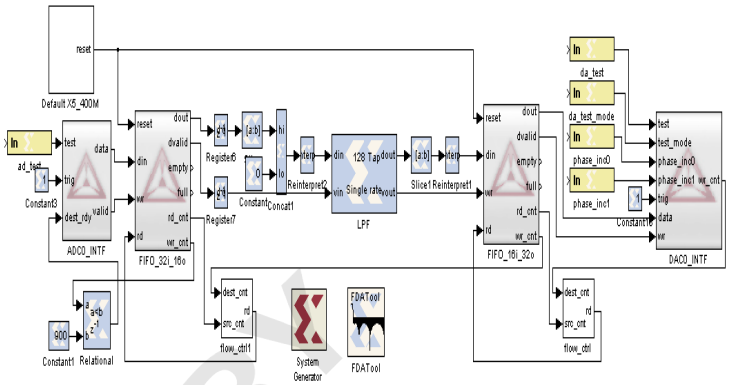
High speed DSP, analysis, customized triggering and other unique features may be added to the X5 modules by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



Using MATLAB Simulink for X5 Logic Design

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools under Xilinx ISE.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

IP for DDC Channelizer Cores

In cooperation with R-Interface, a leading provider of IP cores for wireless applications, a range of down-conversion channelizer logic cores for wideband and narrowband receiver applications is available. When fitted with these cores, the X5 modules provide powerful receiver functionality integrated for IF processing.

The DDC channelizers are offered in channel densities from 16 to 4096. Applications that have equi-spaced channels can have up to 4096 channels in a single X5 card, while wideband applications requiring completely independently channelizers and full programmability for filters can use the 32 or 16 channel version.

All channelizers feature programmable independent channel gains from 0 to 60 dB with 0.07 dB resolution.

Part Number	IP Core	Channels	Tuning	Decimation	Max Bandwidth	Channel Filter
58003	IP-RI-MDDC16	16	Fs/2^33	128 to 65536	Fs/256	Programmable 121 tap filter
58004	IP-RI-MDDC32	32	Fs/2^33	128 to 65536	Fs/256	Programmable 121 tap filter
58006	IP-RI-CHTU 128/256	128 or 256	Fs/2^33	512 to 16384	128 channels: 0.8 *Fs/512 256 channels: 0.8 *Fs/1024	80 dB rejection
58007	IP-RI-CHTU 32/4096	16 to 4096	Fixed, equal spaced channels	Specify at order	Fixed, specify at order	80 dB rejection

Additional IP cores are offered for IF processing and baseband demodulation.

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Part Number	IP Core	Features
58001	PSK Demodulation	N=2,4,8,PI/4. Integrated carrier tracking and bit decision.
58002	FSK Demodulation	Programmable discrimination filters, bit decision logic.
58003	TinyDDC	Tiny DDS, 1/3 size of Xilinx DDS with equal SFDR, clock rates to 400 MHz with flow control
58011	XLFFT	IP core for 64K to 1M FFTs with windowing functions

Applications Information

Cables

The X5-RX module uses coaxial cable assemblies for the analog I/O. The mating cables are SMA male termination with 50 ohm characteristic impedance.

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The X5 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with 16 LVTTL signals provide support for data transfer rates up to 1.6 GB/s sustained, as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed Rocket IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80195 is suitable for high speed P16 applications.

PCIe-XMC Adapter (80172)
x1 PCIe to XMC
Clock and trigger inputs

PCIe-XMC Adapter x8 lane (80173)
x8 PCIe to XMC
x8 RIO ports supported on P16

PCI-XMC Adapter (80167)
64-bit, 133 MHz PCI-X host
x4 PCIe to XMC

Compact PCI-XMC Adapter (80207)
64-bit, 133 MHz PCI-X host
x4 PCIe to XMC
PXI triggers and clock support

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X3 modules. The eInstrument PC hosts two XMC modules and provides an embedded Windows or Linux PC in a compact form-factor. The eInstrument Node hosts a single XMC module in a compact chassis that communicates with the host computer over cabled PCI Express.

X5-RX

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201)

Windows/Linux embedded PC

Low Power Intel Atom or high performance Penryn CPUs

8x USB, GbE, cable PCIe, VGA

High speed x8 interconnect between modules

GPS disciplined, programmable sample clocks and triggers to XMCs

100 MB/s, 400 GB datalogger

12V operation

eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion

Up to 7 meter cable

electrically isolated from host computer

software transparent

X5-RX

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