

# X5-TX

V.0.1 10/27/08



PCI Express XMC Module with Four channels 500 MSPS or Dual 1 GSPS, 16-bit DAC outputs, Virtex5 FPGA with 512MB DDR2 DRAM and 4 MB QDR SRAM Memories

## FEATURES

- 16-bit DACs: Four outputs at 500 MSPS or Two outputs at 1 GSPS
- +/-1V, 50 ohm, DC or AC coupled inputs
- External or internal sample clocking and triggering
- Xilinx Virtex5, SX95T or LX155T FPGA
- 512MB DDR2 DRAM
- 4MB QDR-II SRAM
- 8 Rocket IO private links, 2.5 Gbps each
- >1 GB/s, 8-lane PCI Express Host Interface
- Power Management features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

## APPLICATIONS

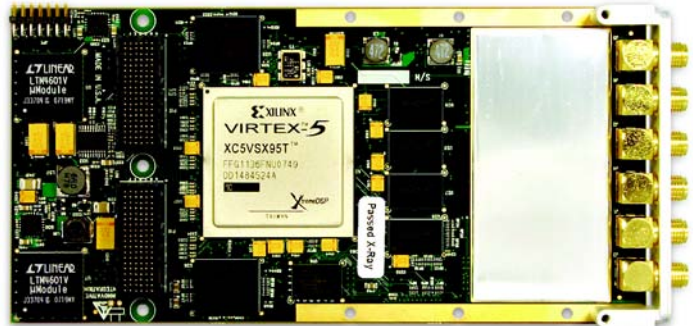
- Wireless Transmitter
- RADAR pulse generation
- High Speed Arbitrary Waveform Generation
- Electronic Warfare
- IP development

## SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ Host Tools

## IP Cores

- Multi-channel N-ary PSK modulator
- Chirp Generator



## DESCRIPTION

The X5-TX is an XMC I/O module featuring four channels of 500 MSPS, 16-bit DAC outputs with a Virtex5 FPGA computing core, DRAM and SRAM memory, and eight lane PCI Express host interface. The DAC devices also support a mode providing two channels at a true 1 GSPS, 16-bit rate without interpolation.

A Xilinx Virtex5 SX95T or LX155T with 512 MB DDR2 DRAM and 4MB QDR-II memory provides a very high performance DSP core for demanding applications such as RADAR and direct RF digitizing. The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at rates exceeding 300 GMAC/s.

The X5 XMC modules couple Innovative's powerful Velocia architecture with a high performance, 8-lane PCI Express interface that provides over 1 GB/s sustained transfer rates to the host. Private links to host cards with >1.6 GB/s capacity using P16 are provided for system integration.

The X5 family can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

IP logic cores are also available for SDR applications that provide multi-channel modulations for PSK and FSK systems. These IP cores transform the X5-TX module into versatile transmitter, ready for integration into your application.

Software tools for host development include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features and use are provided, including streaming DAC samples from disk. The X5-TX can be used with the Andale high speed data record/playback system for arbitrary waveform generation from recorded data at sustained rates exceeding 750 MB/s.



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11/01/08

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# X5-TX



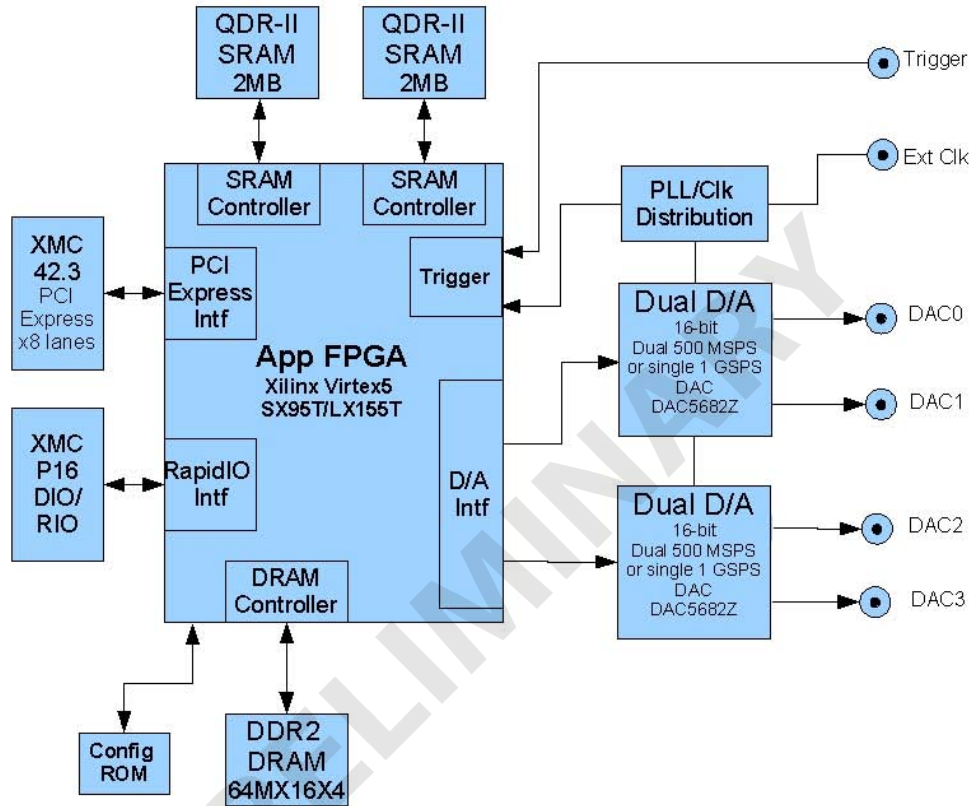
This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

Product	Part Number	Description
X5-TX	80214-0	PCI Express XMC module with four channels of 500 MSPS or two channels 1 GSPS 16-bit DAC, DC-coupled output, Virtex5 SX95T FPGA, 4MB SRAM, 512MB DRAM.
X5-TX	80214-1	PCI Express XMC module with four channels of 500 MSPS or two channels 1 GSPS 16-bit DAC, AC-coupled output, Virtex5 SX95T FPGA, 4MB SRAM, 512MB DRAM.
X5-TX	80214-2	PCI Express XMC module with four channels of 500 MSPS or two channels 1 GSPS 16-bit DAC, DC-coupled output, Virtex5 LX155T FPGA, 4MB SRAM, 512MB DRAM.
X5-TX	80214-3	PCI Express XMC module with four channels of 500 MSPS or two channels 1 GSPS 16-bit DAC, AC-coupled output, Virtex5 LX155T FPGA, 4MB SRAM, 512MB DRAM.
<b>Logic</b>		
X5-TX FrameWork Logic	55027	X5-TX FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
<b>Cables</b>		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
<b>Adapters</b>		
XMC-PCIe x1 Adapter	80172-0	PCI Express Carrier card for XMC PCI Express modules, x1 lanes
XMC- PCIe x8 Adapter	80173-0	PCI Express Carrier card for XMC PCI Express modules, x8 lanes
XMC-PCI Adapter	80167	PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-cPCI Adapter	80207	3U Compact PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
<b>Embedded PC Host</b>		
eInstrument PC	90199	Embedded PC XMC host with support for two XMC modules for standalone applications.

# X5-TX

X5-TX Block Diagram



# X5-TX

## Standard Features

Analog	
Outputs	4
Output Range	DC Coupled: +/- 1V AC Coupled: TBD
Output Type	Single ended DC-coupled (80214-0, -2) AC-coupled (80214-1, -3)
Output Impedance	50 ohm
D/A Device	Texas Instruments DAC5682Z
D/A Resolution	16-bit
D/A Sample Rate	200 to 1000 MHz
D/A Update Rate	1000 MHz maximum
Data Format	2's complement, 16-bit integer
Interpolation	2x,4x options
Coarse Mixer	Fs/4
Connectors	SMA female
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

FPGA	
Device	Xilinx Virtex5 XC5VSX95T-1FF1136C XC5VLX155T-1FF1136C
Speed Grade	-1 (commercial)
Size	SX95T :~9M gate equivalent LX155T :~15M gate equivalent
Flip-Flops	SX95T: 69120 LX155T : 97280
Multipliers	SX95T: 640 LX155T: 128
Slice	SX95T: 17,280 LX155T: 24,320
Block RAMs	SX95T: 296 (5328 Kbits) LX155T: 212
Rocket IO	16 lanes @ 2.5 Gbps
Configuration	SelectMAP from on-board flash EEPROM - JTAG during development

Memories	
DRAM Size	512MB total 4 devices @ 64Mx16 each
DRAM Type	DDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	4.2 GB/s storage/retrieval rate sustained
SRAM Size	4 MB total 2 devices @ 512Kx32 each
SRAM Controller	Two independent SRAM controllers implemented in FPGA logic
SRAM Type	QDR-II
SRAM Rate	1.2 GB/s simultaneous read and write rates, (2.4 GB/s total)

# X5-TX

Host Interface	
Type	PCI Express; 8 lanes
Sustained Data Rate	1 GB/s
Protocol	PCI Express with Velocia packet system
Connector	XMC P15
Interface Standard	PCIe 1.0a; VITA 42.3
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Source	Programmable PLL: AD9510, output sample clock rates to 500 MHz
	External: Sine 10 MHz to 500 MHz, 0.2-2.0Vp-p (-20.8 to -0.8 dBm) AC-coupled, 50-ohm terminated
Jitter	PLL: 200 fs RMS @ 500 MHz External: 50 fs additive, divider = 1, 500 MHz
External Clock Connector	SMA female
Triggering	External, software, play N frame
Trigger Connector	SMA female
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.

Acquisition Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Underflow, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	4 ns resolution, 32-bit counter

P16 Digital IO	
Rocket IO Channels	8
Rocket IO data rate	2.5 Gbps/lane (2 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	16
Signal Standard	LVTTL (3.3V)
Drive	+/-12 mA
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	135g without heatsink
Hazardous Materials	Lead-free and RoHS compliant

# X5-TX

## ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Supply Voltage, VPWR to GND	+4.5	+12.5	V	
Analog Input Voltage, Vin+ or Vin- to GND	-5.7	+5.7	V	DC Coupled
Operating Temperature	0	70	C	Non-condensing, forced air cooling required
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

## RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage	+3.15	+3.3	+3.45	V
Supply Voltage	+11	+12	+13	V
Operating Temperature	0		60	C
Forced Air Cooling	2**	5	-	CFM

# X5-TX

## RECOMMENDED OPERATING CONDITIONS

### ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
Analog Output Bandwidth	TBD	MHz	-3dB
SFDR	TBD	dB	101 MHz sine output, -3 db FS, 20 Hz to 200 MHz, DC coupled
S/N	TBD	dB	101 MHz sine output, -3 db FS, 20 Hz to 200 MHz, DC coupled
THD	TBD	dB	101 MHz sine output, -0.5 db FSR, DC coupled
ENOB	TBD	dB	101 MHz sine output, -3 db FS, 20 Hz to 200 MHz, DC coupled
Channel Crosstalk	TBD	dB	Aggressor = 100 MHz, 1.9Vp-p adjacent channel
Noise	TBD	mV pk-pk	DC output, Fs = 500 MSPS
Noise floor	TBD	dB	DC output
Power Consumption	25	W	All channels sampling at 1500 MSPS, 27C ambient; specific applications may be may vary from 12 to 35W
Gain Error	<0.02	% of FS	Calibrated
Offset Error	<10	mV	Calibrated


# X5-TX

## Architecture and Features

The X5-TX module architecture integrates analog IO with an FPGA computing core, memories and PCI Express host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates making it ideal as a front-end for demanding applications for complex signal generation used in wireless transmitters, RADAR, and electronic warfare applications.

### Analog IO

The analog front end of the X5-TX module has four simultaneously updated channels of 16-bit, 500 MSPS DAC outputs that may be configured to operate as two outputs updated 1 GSPS. The DAC outputs have an analog input bandwidth Nyquist shifting. The DACs are directly connected to the FPGA for minimum data latency. In the standard logic, the DACs have an interface component that sources the data and provides digital error correction. The digital error correction is used to compensate for gain and offset errors on a sample-by-sample basis in the logic. This method is more stable than analog adjustments and typically sacrifices less than 1% of the analog range. A non-volatile ROM on the card is used to store the calibration coefficients for the analog and is programmed during factory test.

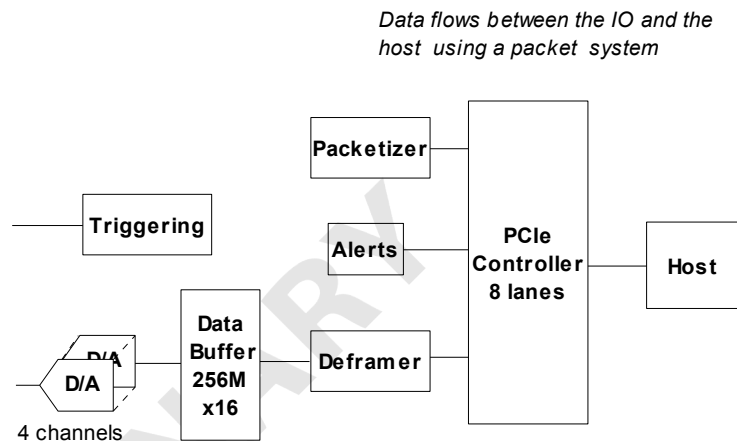
The DAC channels operate synchronously for simultaneous DAC updates using either the PLL or an external clock input. Controls for triggering allow precise control over the playback of data and are integrated into the FPGA logic. Trigger modes include frames of programmable size, external and software. Multiple cards can play simultaneously by using external trigger inputs and clock. The trigger component in the logic can be customized to accommodate a variety of triggering requirements.

### FPGA Core

The X5 Module family has a Virtex5 FPGA and memory at its core for DSP and control. The Virtex5 FPGA is capable of  $>300 \times 10^9$  MACs (SX95T operating at 500 MHz internally), about 20x faster than traditional DSPs. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to 512MB of DDR2 DRAM capable of  $>4$  GB/s data transfer rate and an two independent banks of 2MB QDR SRAM capable of 4GB/s data rate each. These memories are used as FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for waveform calculations. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The X5 module family uses the Virtex5 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X5 module functionality.

### PCI Express Host Interface



**X5 Architecture**

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The X5 architecture delivers over 1 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data to the DACs, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and disassembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex5 FPGA using 8 Rocket IO ports, for a maximum bit rate of over 20 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 200 MB/s per lane. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

## Private Data Links

The X5 module family has private data links on the P16 connector that can be used for system integration. The P16 connector has 8 Rocket IO links each capable of 2.5 Gbps and 16 sideband signals. The 8 RIO lanes can be used to provide low-latency, high rate data to the system in addition to the PCI Express interface. Maximum data rates, with deterministic performance can be implemented in performance-driven systems using little or no protocol. For more complex systems, protocols such as Aurora can be used.

## Module Management

The data acquisition process can be monitored using the X5 alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the X5 cards easier to integrate into larger systems.

## FPGA Configuration

The X5 modules have a 128Mb FLASH that holds two FPGA application images. In addition to the application image, a “golden” image is kept in FLASH for disaster recovery. The FLASH can be reprogrammed in-system using a software applet for field upgrades.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx cables such as Platform USB and Parallel IV Cable.

## Software Tools

Software development tools for the X5 modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

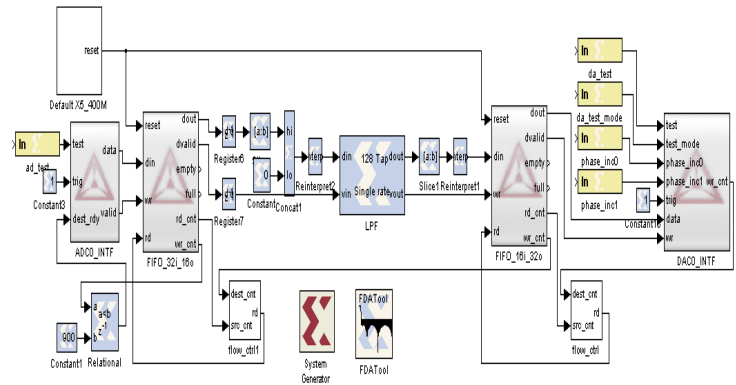
Example software for data playback and card control are provided with every X5 module. Data can be played back from system memory at full rate or from disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the X5 performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

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Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

## Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the X5 modules by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



*Using MATLAB Simulink for X5 Logic Design*

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

## Applications Information

### Cables

The X5-TX module uses coaxial cable assemblies for the analog IO. The mating cable should have an SMA male connector and 50 ohm characteristic impedance for best signal quality.





### XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.


The X5 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with 16 LVTTTL signals provide support for data transfer rates up to 1.6 GB/s sustained, as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed Rocket IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80195 is suitable for high speed P16 applications.

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<p><b>PCIe-XMC Adapter (80172)</b>  x1 PCIe to XMC  Clock and trigger inputs</p> 	<p><b>PCIe-XMC Adapter x8 lane (80173)</b>  x8 PCIe to XMC  x8 RIO ports supported on P16</p> 	<p><b>PCI-XMC Adapter (80167)</b>  64-bit, 133 MHz PCI-X host  x4 PCIe to XMC</p> 	<p><b>Compact PCI-XMC Adapter (80207)</b>  64-bit, 133 MHz PCI-X host  x4 PCIe to XMC  PXI triggers and clock support</p> 
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Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X3 modules.

<p><b>eInstrument PC with Dual PCI Express XMC Modules (90199)</b>  Windows/Linux embedded PC  8x USB, GbE, cable PCIe, VGA  High speed x8 interconnect between modules  GPS disciplined, programmable sample clocks and triggers to XMCs  100 MB/s, 400 GB datalogger  12V operation</p> 	<p><b>eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)</b>  PCI Express system expansion  Up to 7 meter cable  electrically isolated from host computer  software transparent</p> 
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# X5-TX

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