

Conejo

Four Analog I/O Channels
Up to 10MHz input/50MHz output
900 MFLOPS Floating Point DSP
TMS320C6711 150MHz

Features

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|--|
| 150MHz TMS320C6711 DSP (floating point) |
| 32MB SDRAM |
| 4 Channels 10 MHz, 14-bit Input |
| 4 Channels 15 MHz, 2/30 or 1/50, 16-bit Output |
| 64/32 bit PCI, 33 MHz, 5V/3.3V |
| Supports complex trigger modes with hardware event logging |
| Multiboard Synchronization (ClkLink, SyncLink) |

Applications

| |
|---------------------------------------|
| Wireless & Broadband Hardware Testing |
| Ultra-Fast Flexible Data Acquisition |
| Video Processing |
| Semiconductor Testing |
| RADAR |
| Electronic Warfare |
| Agile Waveform Generation |
| Ultrasound |

Hardware Options

| | |
|---------------------|--------|
| FIFOCable | pg 130 |
| 50 Ohm SMB to BNC | pg 132 |
| CodeHammer Debugger | pg 102 |

Software Development Tools

| | |
|-------------------------|--------|
| Pismo Toolset | pg 96 |
| Armada Toolset | pg 101 |
| TI Code Composer Studio | pg 89 |

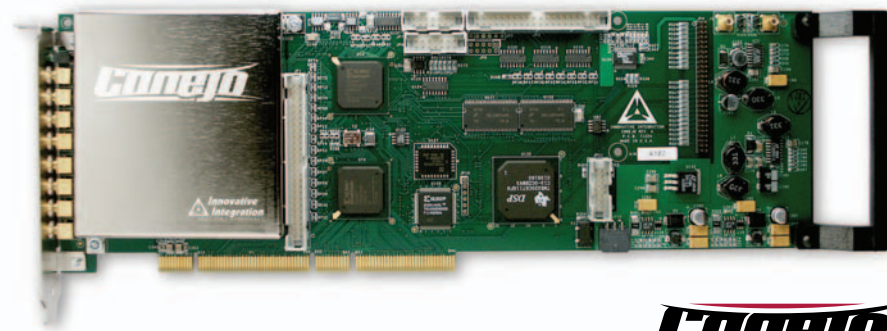
Ordering Information

| | |
|----------------|---------|
| Conejo | 80070-0 |
| Conejo DevPack | 90070-0 |



DevPack Available

See page 91 for details



Overview

Conejo is a performance-oriented DSP card for PCI-based data acquisition, playback and co-processing with four analog I/O channels at up to 10MS/sec input and up to 50MS/s output. It uses the acclaimed C6711 processor from Texas Instruments as the heart of data movement and processing functions. Conejo provides four simultaneous analog inputs, four analog outputs, a logic architecture that supports extremely flexible trigger mechanisms, a choice of timebase sources and a valuable real-time event log. With Innovative Integration's multi-board support features, Conejo is a truly complete solution for a wide array of applications like RADAR, advanced medical imaging, physics research, video processing, semiconductor testing, transient capture, arbitrary waveform generation, industrial scanners, wireless development, precision instruments, ultrasound, etc. The Conejo board shares many features with other boards in the Matador product line. These features are presented in more detail in the overview section of the Matador Series.

Processing Core

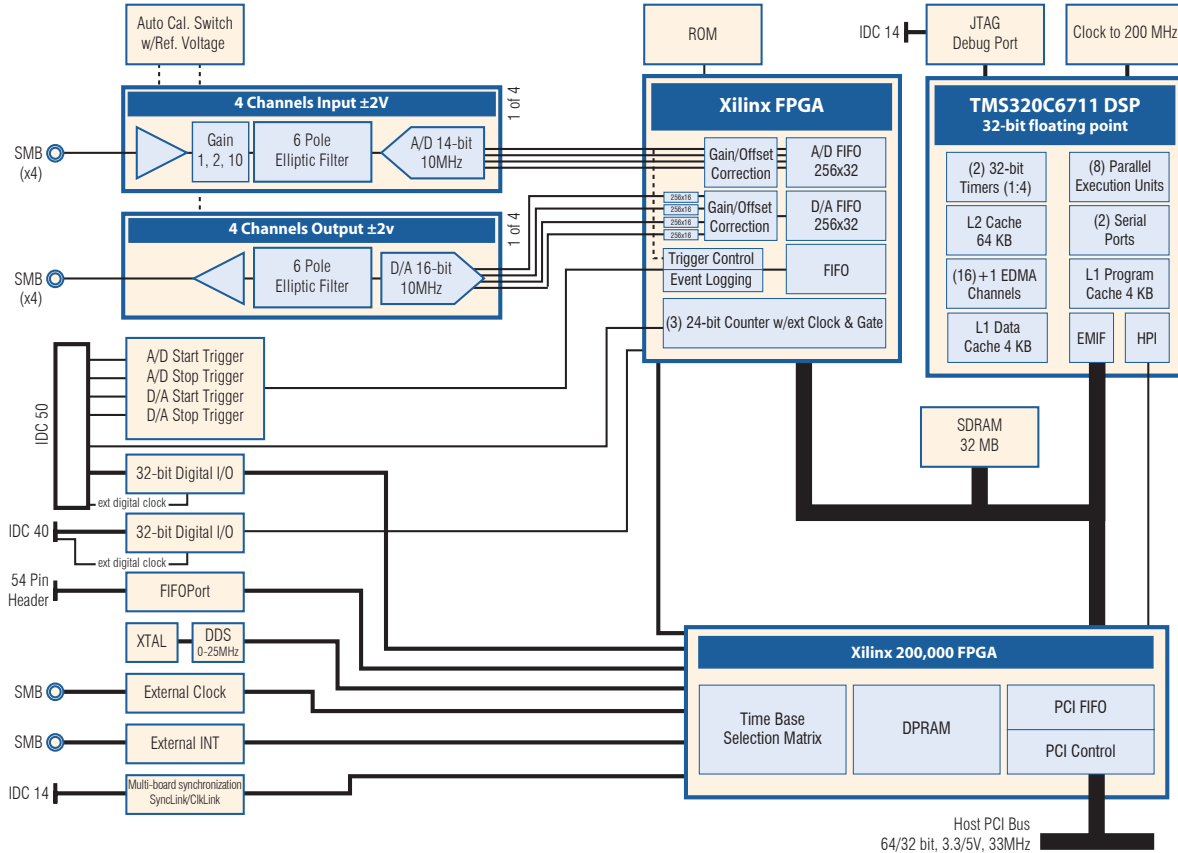
Conejo is powered by one TMS320C6711 DSP, using the proven, highly parallel architecture of the C6000 series of floating-point DSPs from Texas Instruments. The C6711 offers 900MFLOPS of processing power at 150MHz. On-chip resources include 8 highly independent parallel execution units, 16 EDMA channels, two 32-bit timers and an efficient L1/L2 cache controller to achieve near on-chip performance.

Analog Input Channels

Conejo features four independent channels of 14-bit, A/D conversion up to 10MHz. The front-end consists of a single-ended input range of $\pm 2V$ (custom ranges available) into a 50 Ohm input impedance, 6-pole elliptic anti-alias filter with -3dB roll-off set at 5MHz (custom filter available) connected to Analog Devices AD9240 14-bit converter. This converter delivers data from a pipeline that is only 4 samples deep and thus provides low data latency. Data from all channels is written to a FIFO buffer integrated in logic with programmable fill level interrupts. This can provide ample buffering for complex streaming applications or deliver the lowest latency for control systems. An optional decimation function—software programmable with ratio up to 4096—can further reduce latency, allowing to run converters at max speed while delivering data at a lower rate. Gain and offset digital correction is performed within the logic to minimize analog errors. Correction coefficients are saved in non-volatile ROM and may be updated in the field if required. Conversion clock source is defined in logic and can be independent from output conversion.

Analog Output Channels

The output channels consist of a common FIFO buffer 256x32 followed by a digital gain and offset error correction stage feeding four independent DAC FIFOs 256 x 16, all integrated in logic within only one clock latency and delivering four individual data stream to the 16-bit Linear Technology LT1668 converters. These converters are capable of 50MS/s and the firmware allows the programmer to select a few configuration, based on the 300MB/s bus bandwidth: 4 channels at 15MS/s each, 2 channels at 30MS/s each or a single channel at the full 50MS/s. The LT1668 D/A features unmatched AC performance that is ideal for communications applications and



precision waveform generation. The D/A channels are also DC accurate with low glitch energy for control applications. The 6-pole elliptic reconstruction filters provide smooth output and eliminate high-frequency artifacts. The outputs are single-ended and matched to 50 Ohms with a standard range of $\pm 2V$ (custom range available). Conversion clock source is defined in logic and can be different than the input conversion clock.

Time Base, Trigger Modes and Servo-control features

The fields of application for Conejo are endless because of the flexible time bases and the wide choice of trigger mechanisms. Conejo offers a software configurable time base matrix that allows to drive any time base from a choice of clock sources: on-chip and off-chip timers, DDS, external clock, SyncLink/ClockLink. The selection is simply made with single-line SW commands.

The trigger methods are extremely flexible and accommodate almost any foreseeable synchronization requirements. Conejo can quickly be configured for any of the following methods and attributes: external trigger, analog threshold trigger, continuous streaming, framed acquisition (specified by timer or sample counter), pre/post trigger sampling, counted or timed frames, re-trigger mode. Any trigger register, from timer to analog threshold, can be shared between cards using the SyncLink/ClockLink interface. Please refer to the Matador overview for more details on triggering modes.

Finally, Conejo offers two built-in logic features designed specifically for closed-loop control. An input decimation mode allows to discard a programmable number of A/D samples for every sample saved for processing. By “tuning” the decimation ratio, the developer can adjust the interrupt rate driving his control loop while obtaining the lowest latency on A/D readings. On the output side, an automatic DAC update feature allows to write to DAC’s at a programmable delay from the A/D conversion: this minimizes output latency, provides a fixed frequency D/A update and reduces CPU interrupts. FIFO overrun/underrun registers can be read during development to facilitate timing optimization.

Expansion and Multi-Card Synchronization

Conejo’s FIFOPort offers high-speed dedicated parallel board-to-board communication between multiple Conejo cards and other FIFOPort compatible cards at rates to 50 MBytes/sec.

Conejo provides other features that make system-level integration fast and easy, such as SyncLink/CikLink for multiple card synchronization and Plug-n-Play

PCI. The SyncLink/CikLink interface allows up to four unique timing signals and event triggers to be shared between up to 16 cards. Each Conejo card has a switch matrix that routes any event trigger to any SyncLink/CikLink port, completely under software control. There is no complex cabling, just a simple connection and software configuration.

Host PC Interface

The Conejo card features a 64 bit PCI bus interface capable of busmastering data bursts up to 264 Mbytes/sec. This PCI interface automatically accommodates 64bit/32bit and 3.3V/5V PCI buses running at 33 MHz and configures itself at power-up. The PCI interface built in the firmware manages all busmastering activities independent of the DSP and greatly reduces the complexity of integrating the Conejo into host computer applications. Data simply appears in host memory, ready for use by the host program, all at great speed with low latency. Benchmarks of 80MBytes/sec of sustained transfer rates on 32-bit busses have been demonstrated under Win2K. But the most attractive aspect is that these high rates are achieved with no burden at all on the target (i.e. 0% CPU utilization and only 25% bus utilization).

An arbitrated, 16 word dual-port RAM is also provided and is useful for data passing and general communication. This dual-port memory serves a mailbox, or bulletin board, where the DSP and host can swap status and data structures with minimum interference.

Development Tools

First time buyers of Conejo will need to purchase the Conejo DevPack. The DevPack includes the Conejo card, Code Composer Studio Integrated Development Environment, CodeHammer JTAG Emulator and the Pismo Toolset for Conejo.

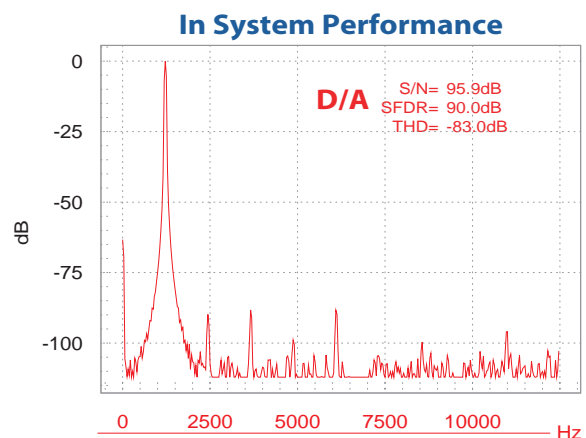
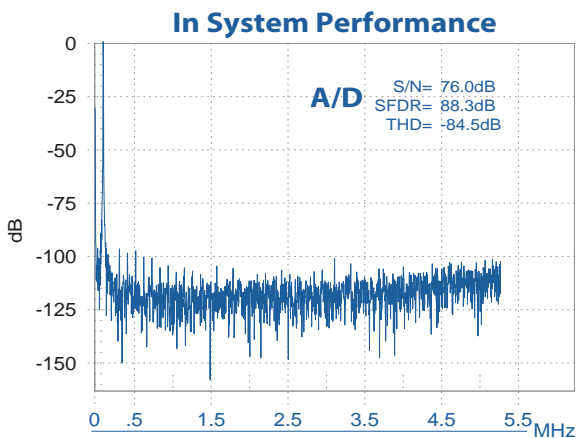
Innovative Integration's Pismo Toolset makes DSP development fast and simple with a complete collection of target and host side libraries. The Pismo Toolset includes everything from convenient utility applets allowing download, execution and high level debugging of DSP applications to a complete set of source code examples demonstrating full operation of Conejo. The Pismo Toolset is fully supported from within Texas Instruments' Code Composer Studio. Pismo supports and extends each of the features of DSP/BIOS on Conejo through a seamless integration of advanced C++ class libraries, BIOS-compliant DSP peripheral device drivers, and clear, illustrative examples. The device drivers fully exploit the available DMA channels in the C6711 chip so that hardware interrupt rate rarely exceeds one kHz! The net effect is that virtually all of the bandwidth of the CPU is available for application processing.

Host side development is accomplished with Armada. This advanced set of tools is integrated into either Borland C++ Builder or Microsoft Visual C++ and offers the most powerful and flexible means to rapidly integrate real time video signal processing into Windows applications. Armada includes a set of visual software components for the Borland C++ Builder Environment, or C++ objects for Visual C++ allows development of simple-yet powerful application programs capable of exploiting the full power of Conejo including efficient data movement synchronized with the target code, viewing/graphing, signal post-processing or analysis, and disk logging. Host side data streaming and viewing example programs are provided.

OEM Configurations

Conejo can be configured to fit your specific requirements and provide an optional mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.

64bit PCI DSP



Digital Signal Processor

Texas Instruments' TMS320C6711
150MHz
32-bit floating point DSP
4Kbytes L1 program & 4Kbytes L1 data cache
64Kbytes L2 cache, partitionable for PRAM
16 EDMA channels
Two 32-bit timers

Debug Port

JTAG 1149.1 compliant emulation port
Compatible with Code Hammer, XDS-510
or equivalent debugger using CCStudio

Memory

32 Mbytes SDRAM (1 wait state)
256 word dual port RAM

PCI Bus

64/32 bit, 3.3/5V, 33MHz
Capable of 264/132Mbytes/sec respectively
Controller auto-detects host bus type at Plug-n-Play
Busmaster or slave operation
FIFO and dual port memory interface
Requires 1Mbyte host memory space

Digital I/O

64 bits, distributed in 2 banks of 32 bits
Programmable as input or output in groups of 8
TTL compatible with ± 24 mA capability

FIFOPort

50Mbytes/s bi-directional external data port
32-bit interface to DSP
256x32 FIFO memory
Requires FIFOCable for LVDS drive

Timers/Counters

Two 32-bit on-chip timers/counters
Timer input: onboard 80MHz crystal or
External clock or SyncLink
Three 24-bit timers in logic

Timebase & Triggers

Conversion timebase is selectable from DDS,
5 timers, External clock, SyncLink/ClockLink and
is independent between A/D and D/A.
Automatic DAC convert on programmable delay
from A/D convert for servo applications
Start & Stop triggers are selectable from timers,
external clock, SyncLink/ClockLink, software
command
Or Programmable acquisition duration from start
can be specified with time or sample count
Real-time trigger and conversion event logging
built in logic

Multi Card Synchronization

SyncLink/ClockLink will share
6 signals (5 TTL + 1 LVDS pair) between boards
to synchronize timebase and trigger events

Analog Input

4 simultaneous channels, 14-bit,
0 to 10MHz
Analog Devices AD9240 converter
6-pole anti-alias elliptic filters
-3dB rolloff @ 5MHz, -120dB/decade
Input range ± 2 V, ± 1 V, ± 0.2 V (sw programmable)
DC-coupled Single-ended input, 500hm
impedance
256 samples FIFO
Digital gain & offset error correction in logic
Latency A/D to DSP: 4 samples + 0.5 μ sec

Analog Output

4 simultaneous channels, 16-bit, 0 to 15 MHz
or 30 MHz for two channels or 50MHz for one channel
Linear Tech LTC1668 converter
6-pole reconstruction elliptic filters
-3dB rolloff @ 5MHz, -120dB/decade
Output range ± 2 V
Single-ended output matched to 50 Ohm
impedance
DC-coupled Dual stage FIFO with 256 samples/
ch
Digital gain & offset error correction in logic
Stack mode allows 25MHz/2ch. or 50MHz/1ch.
Latency DSP to DAC: 0.5 μ sec

Timebase Sources

Programmable DDS 0-25MHz in 0.02Hz steps
External Clock
SyncLink/ClockLink
DSP Timers

Connectors

A/D - SMB
D/A - SMB
32-bit digital I/O, start/stop triggers - IDC50
32-bit digital I/O - polarized IDC40
FIFOPort - 54 pin 2mm header
SyncLink/ClockLink - polarized IDC10
Two Sync serial ports (McBSP) - polarized
IDC10
JTAG - polarized IDC14
External clock - SMB
External trigger - SMB

Physical Size

Full Size PCI card
Max component height: 13mm

Power requirements

+5V @ 1A; +12V @ 0.5A

Operating Temperature

10^o-55^o C

Development Environment

DSP
C, C++ , assembler using TI CCStudio and
Pismo Toolset
Host PC
Borland Builder C++ , Microsoft VC++

Operating System

DSP/BIOS II



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Software Selection Guide for Conejo

| Software Package | Description | Usage/Requirements | Page | Recommendations |
|------------------------|--|---|------|--|
| Pismo Toolset | Peripheral libraries needed for developing code on this card. Includes host applications and target examples in source form demonstrating use of peripherals on the card, DSP/BIOS peripheral device drivers. | Requires CCStudio*. Win2000/XP compatible. | 98 | Required for all first time users. Includes 1 year of technical support. |
| Caliente DLL | Dynamic link library (DLL) for the Conejo. | Requires ANSI-compliant C/C++ compiler. For example, Microsoft Visual C/C++. Win2000/XP compatible. | | Required for interfacing Host side code to DSP. May be used without Armada although not recommended |
| CCStudio 'C6000 | Integrated development environment (IDE) for Target side development/debugging from Texas Instruments. | Requires XDS-510 compatible JTAG emulator for debugging capabilities. | 91 | Required for all first time users. Recommend use with Innovative Integration plug-n-play PCI JTAG emulator. |
| Armada | Host side development package using a revolutionary integrated development environment (IDE). Allows user to build/debug sophisticated data acq apps fully using MS Windows graphical environment quickly with Innovative Integration's Visual Component Libraries (VCL) of MFC Classes. | Requires Borland C++ Builder* or Microsoft Visual C++. | 103 | Recommended for inexperienced and seasoned C/C++ programmers. Offers easiest interface while providing the most flexibility and performance. Ties into a plethora of 3rd party components. |

The Conejo Development Package contains all software packages listed above.

*Contact Innovative Integration for current release version.