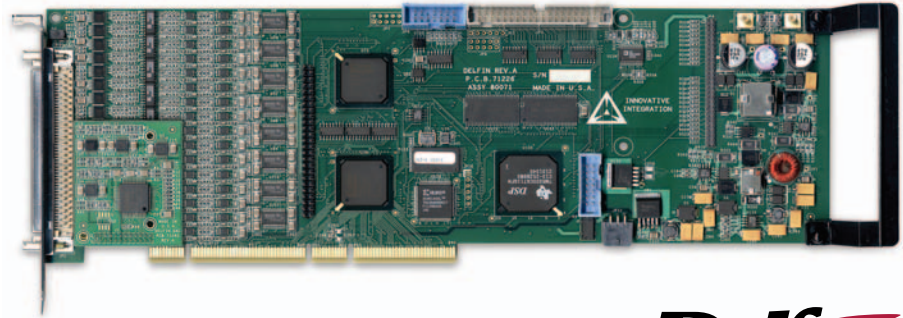


Delfin

32 A/D Channels & 6 D/A Channels
24-bit, Sigma-Delta, 192 kHz
100+ dB SFDR & THD
Choice of Software Tools



Delfin

Features

150MHz TMS320C6711 DSP (floating point)
32 Simultaneous A/D up to 192 kHz, 24-bit Input (16 & 8 input channel configurations available)
6 Channels, 192 kHz, 24-bit Output
64/32 bit PCI, 33 MHz, 5V/3.3V
Multiboard Synchronization (ClkLink, SyncLink)
Supports complex trigger modes
Supports all standard audio rates
Exceptional Software Support

Applications

SONAR
Vibration Analysis & Monitoring
Acoustic Monitoring & Control
Professional Audio
Precision Instruments

Hardware Options

FIFOCable	pg 130
100 Pin MDR Breakout	pg 131
CodeHammer Debugger	pg 102

Software Development Tools

Turnkey Applications	
Graphical Programming	
Pismo Toolset	pg 98
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TI Code Composer Studio	pg 91

Ordering Information

Delfin-32 A/D channels	81071-1
Delfin-16 A/D channels	81071-2
Delfin-8 A/D channels	81071-3



DevPack Available

See page 91 for details

Overview

Delfin is a performance-oriented DSP card for PCI-based data acquisition, playback and coprocessing with a high channel count of analog I/O using sigma-delta converters up to 192kHz. It provides up to 32 simultaneous analog input and 6 analog output, both at 24-bit resolution and using the highest quality analog circuitry to deliver a spectral-free dynamic range exceeding 100dB. It is designed around the acclaimed C6711 processor from Texas Instruments, which acts as the data movement and processing center. The state-of-the-art logic architecture supports flexible trigger mechanisms and a choice of timebase sources. Combined with Innovative Integration's multi-board support features, Delfin is a truly complete solution for a wide array of applications like professional audio, advanced sonar, vibration analysis, acoustic-based aerodynamics, precision instruments. The Delfin board shares many features with other boards in the Matador product line. These features are presented in more details in the overview section of the Matador Series.

Processing Core

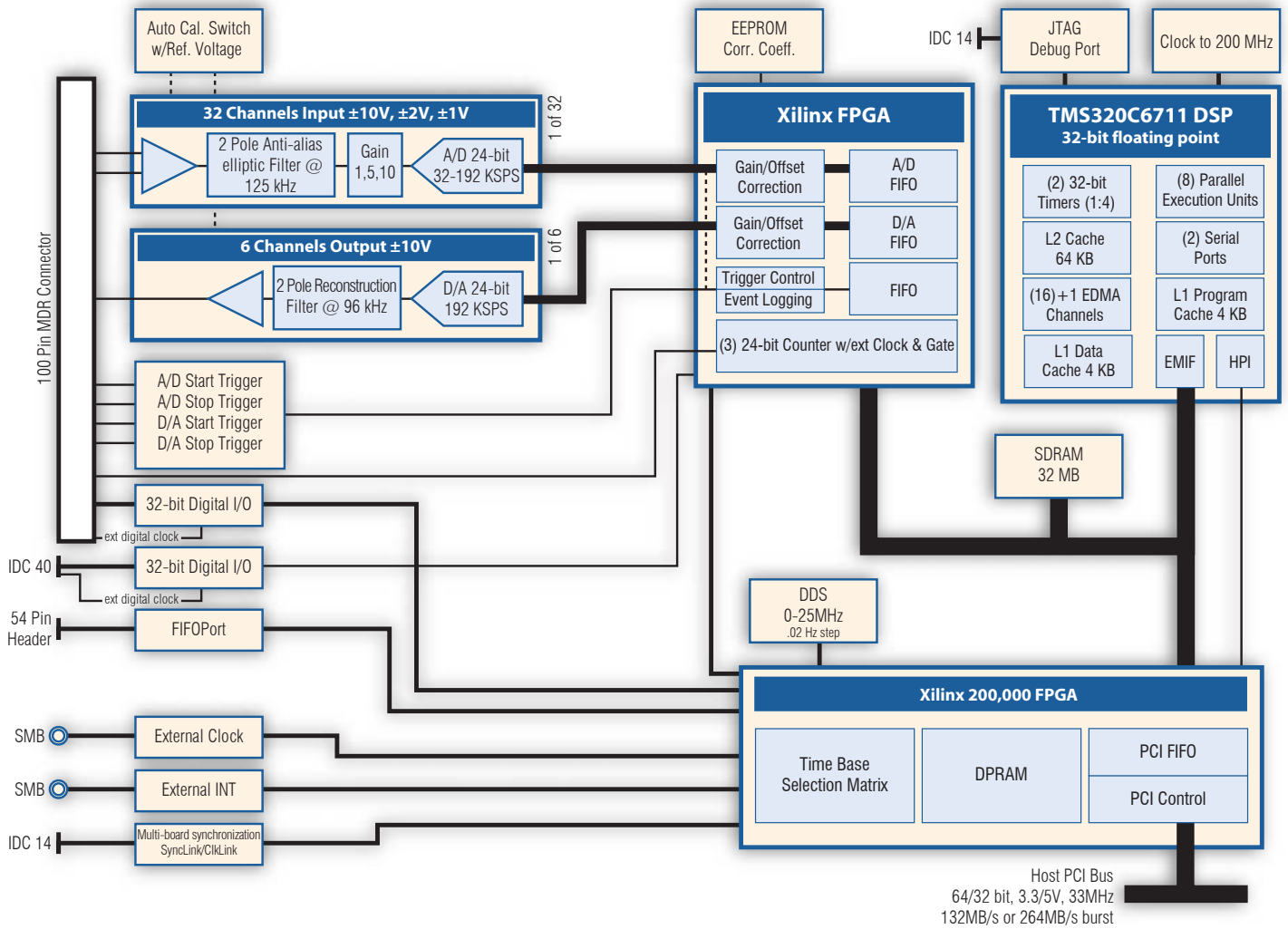
Delfin is powered by one TMS320C6711 DSP, using the proven, highly parallel architecture of the C6000 series of floating-point DSP's from Texas Instruments. The 6711 offers 900 MFLOPS of processing power at 150MHz. On-chip resources include 8 highly independent parallel execution units, 16 EDMA channels, two 32-bit timers. Memory on Delfin includes 32 MB of 1WS SDRAM and utilizes the on-chip L1/L2 cache controller to achieve near on-chip performance.

Analog Input Channels

Delfin features 32 independent channels of 24-bit, sigma-delta A/D conversion with sampling rate ranging from 32 to 192kHz. Boards configuration with a lower channel count of 16 or 8 are also available. The front-end consists of high impedance differential input in range of $\pm 10V$, $\pm 5V$ or $\pm 1.25V$ (custom ranges available), into a 2-pole elliptical anti-alias filter with -3dB rolloff set at 125kHz (custom filter available). Each pair of input signals is connected to a Burr-Brown PCM1804 stereo converter. This is a high-performance converter that uses a precision sigma-delta modulator for over-sampling and includes a linear phase anti-alias digital decimation filter. Two modes of over-sampling are supported (128X or 256X), each offering different filter characteristics and analog performance. In all modes, the pipeline group delay is 37/fs. This means start-up conditions yield a first 37 "bad" samples, and this build-in latency of 37 samples can render the converter architecture inadequate for low latency applications such as closed-loop servo control. The inputs are DC-coupled as factory default but a lowcut filter can be enabled via software to remove the DC offset component. The converter architecture offers incredible dynamic range and SFDR performance beyond 100dB. Data from all channels are written to a 512x32 FIFO buffer integrated in logic with programmable fill level interrupts. Gain and offset digital correction is performed within the logic and correction coefficients are saved in non-volatile ROM and can be updated in the field.

Analog Output Channels

The D/A sampling frequency is between 10kHz and 192 kHz, but must be the same as the A/D conversion clock. The output channels consist of a common FIFO buffer 512x32 splitting into six individual streams of 24-bit data into the digital gain and offset error correction stage integrated in logic and feeding the six independent channels of the PCM1604 digital-to-analog



converter. This converter incorporates a digital interpolation filter and a multi-level, sigma-delta modulator that employs 4th-order noise shaping and 8-level amplitude quantization followed by an analog low pass filter to achieve excellent signal-to-noise performance. Built-in delay time is 34/fs. Similarly to the A/D, this long latency may not be adequate for fast closed-loop control applications. The converter output is amplified and fed through a 2-pole elliptic filter with -3dB roll-off at 96kHz for an output range of $\pm 10V$ that is DC accurate (custom ranges available). This DAC also offer special features that are all controlled on Delfin via one McBSP serial port: digital attenuation, soft mute, zero-detect, de-emphasis, filter roll-off sharpness, etc.

Time Base and Trigger Modes

The fields of application of Delfin are wide because of the flexible time bases and the wide choice of trigger mechanisms. Delfin offers a software configurable time base matrix that allows the user to select the time base input from a choice of clock sources: DDS, external clock, SyncLink/ClockLink. The selection is simply made with single-line SW commands. The trigger methods are extremely flexible and accommodate almost any foreseeable synchronization requirements. Delfin can quickly be configured for any of the following methods and attributes: external trigger, analog threshold trigger, continuous streaming, framed acquisition (specified by timer or sample counter), pre/post trigger sampling, counted or timed frames, re-trigger mode. Any trigger register, from timer to analog threshold, can be shared between cards using the SyncLink/ClockLink interface. A real-time event logger built in logic on both A/D and D/A stages provides the user with a precision record of various events such as trigger times, data integrity monitoring and user-defined events. Please refer to the Matador overview for more details on triggering modes. Users should keep in mind that sigma-delta converters have higher latency and lengthy digital pipelines.

Expansion and Multi card Synchronization

Delfin's FIFOPort offers high-speed dedicated parallel board-to-board communication between multiple Delfin cards and other FIFOPort compatible cards at rates to 50 MBytes/sec.

Delfin provides other features that make system-level integration fast and easy, such as SyncLink/ClockLink for multiple card synchronization and Plug-n-Play PCI. The SyncLink/ClockLink interface allows up to six unique timing signals and event triggers to be shared between up to 16 cards. Each Delfin card has a switch matrix that routes any event trigger to any SyncLink/ClockLink port, completely under software control. There is no complex cabling, just a simple connection and software configuration.

Host PC Interface

The Delfin card features a 64 bit PCI bus interface capable of busmastering data bursts up to 264 Mbytes/sec. This PCI interface automatically accommodates 64bit/32bit and 3.3V/5V PCI buses running at 33 MHz and configures itself at power-up. The PCI interface built in the firmware manages all busmastering activities independent of the DSP and greatly reduces the complexity of integrating the Delfin into host computer applications. Data simply appears in host memory, ready for use by the host program, all at great speed with low latency. Benchmarks of 80MBytes/sec of sustained transfer rates on 32-bit busses have been demonstrated under Win2K. But the most attractive aspect is that these high rates are achieved with no burden at all on the target (i.e. 0% CPU utilization and only 25% bus utilization).

An arbitrated, 16 word dual-port RAM is also provided and is useful for data passing and general communication. This dual-port memory serves a mailbox, or bulletin board, where the DSP and host can swap status and data structures with minimum interference.

Development Tools

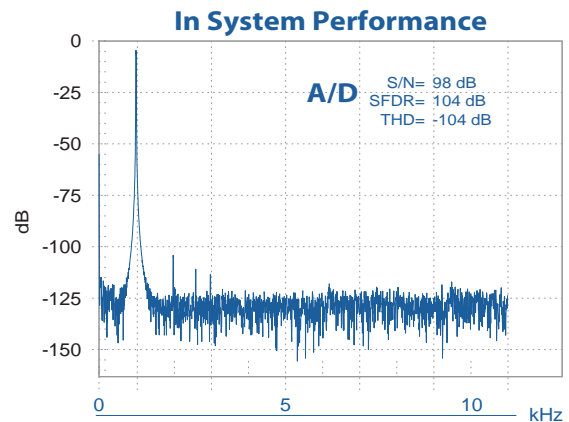
First time buyers of Delfin need to purchase the Delfin DevPack, which includes the Delfin card, Code Composer Studio Integrated Development Environment, Code Hammer JTAG Emulator and the Pismo Toolset.

Innovative Integration's Pismo Toolset makes DSP development fast and simple with a complete collection of target and host side libraries. The Pismo Toolset includes everything from convenient utility applets allowing download, execution and high level debugging of DSP applications to a complete set of source code examples demonstrating the full operation of Delfin. The Pismo toolset is fully supported from within Texas Instruments' Code Composer Studio. Pismo supports and extends each of the features of DSP/BIOS on Delfin through a seamless integration of advanced C++ class libraries, BIOS-compliant DSP peripheral device drivers, and clear, illustrative examples. The device drivers fully exploit the available DMA channels in the C6711 chip so that hardware interrupt rate rarely exceeds one kHz! The net effect is that virtually all of the bandwidth of the CPU is available for application processing.

Host side development is accomplished with Armada. This advanced set of tools is integrated into either Borland C++ Builder or Microsoft Visual C++ and offers the most powerful and flexible means to rapidly integrate real time video signal processing into Windows applications. Armada allows development of simple-yet powerful application programs capable of exploiting the full power of Delfin including efficient data movement synchronized with the target code, viewing/graphing, signal post-processing or analysis, and disk logging. Host side data streaming and viewing example programs are provided.

OEM Configurations

Delfin can be configured to fit your specific requirements and provide an optional mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.



Digital Signal Processor

Texas Instruments TMS320C6711
 150/200 MHz
 72 Kbytes on-chip program/data memory with efficient L1/L2 cache controller
 Two 32-bit timers
 16 DMA channels

Memory

32 Mbytes SDRAM (one wait-state)
 256 Word dual port RAM with host

Debug Port

JTAG 1149.1 compliant emulation port
 Compatible with Code Hammer, XDS-510 or equivalent debugger using TI Code Composer Studio

PCI bus

64/32 bit, 3.3/5V, 33MHz
 Interface auto-detects slot type for configuration
 Capable of 264 Mbytes/sec data rates on 64 bit busses, 132 Mbytes/sec data rates on 32 bit busses
 Busmastering or slave interface
 FIFO and dual port memory interfaces
 Requires 1MB host memory space

Digital I/O

64 bits programmable as input or output in groups of 8, TTL compatible with 24 mA capability

FIFOPort

50 Mbytes/sec bidirectional data path 256x32 FIFO memory
 16-bit data path 32-bit interface to the DSP (requires FIFO cable for proper operation for LVDS signal conditioning)



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Timers/Counters

Two on-chip 32-bit timer/counters
 80 MHz crystal, external clock, or SyncLink
 Three additional 24-bit timers in logic

Analog I/O

A/D
 32 independent ch. of 24-bit A/D converters using TI PCM 1804
 Sampling rate: 32 kHz to 192 kHz
 2 pole elliptic anti-alias filter - 3dB @ 125 kHz
 DC-coupled (default) or AC-coupled
 Differential Input
 Group Delay = 37/fs

A/D Input Range
 SW programmable ±10V, ±5V, ±1.25V
 All-digital offset & gain error correction in FPGA
 512 sample FIFO

D/A
 6 independent ch. of 24-bit D/A converters using TI PCM 1604
 Sampling rate: 10 kHz to 200 kHz
 2 pole reconstruction filter - 3dB @ 96 kHz
 Delay Time = 34/fs

D/A Output Range
 ±10V(custom available for OEMs)
 All-digital offset & gain error correction in FPGA
 512 sample FIFO

Multi-Card Synchronization

Synchronize multiple cards with common trigger or clock
 Five TTL compatible signals (master or slave)
 One high speed LVDS signal for clocks

Time Bases and Trigger Methods

Conversion Timebase
 DDS - 0-25 MHz in 0.02 Hz steps, Two timers, SyncLink/ClockLink, External Clock

Start/Stop Triggers
 External clock, SyncLink, Software Programmable timed duration or sample count
 Conversion real-time event logging in firmware

Connectors

MDR100: Analog I/O triggers, 32-bit digital I/O
 14 pin shrouded, polarized male IDC: JTAG
 54 pin 2mm header: FIFOPort
 40 pin shrouded, polarized male IDC: 32-bit digital I/O
 10 pin shrouded, polarized male IDC: SyncLink/CIKLink
 SMB: External clock and trigger inputs

Physical card size

Full Size PCI card
 Conforms to PCI specification
 Max component height: 10mm

Power Requirements

+5V @ 3.6A (32ch) @ 2.7A (16ch) @ 2.2A (8ch)

Operating Conditions

10°-55° C

Development Languages

DSP
 C/C++ or Assembler using TI Code Composer studio and Pismo Toolset
 PC
 MS VC++, Borland C++ Builder

Operating Systems

Target
 DSP/BIOS II
 Host
 Windows2000, WindowsXP, Red Hat Linux

TMS320C6711 Benchmarks @ 150 MHz

Benchmark Algorithm	Speed
1024 Point Complex FFT (Radix 4, with reversal)	115µsec
FIR Filter (per tap)	13nsec
IIR Filter (per biquad)	27nsec
Matrix Multiply [3x3] * [3x1]	446nsec
[4x4] * [4x1]	800nsec
Divide (y/x)	187nsec
Inverse Square Root	227nsec

Software Selection Guide for Delfin

Software Package	Description	Usage/Requirements	Page	Recommendations
Pismo Toolset	Peripheral libraries needed for developing code on this card. Includes host applications and target examples in source form demonstrating use of peripherals on the card, DSP/BIOS peripheral device drivers.	Requires CCStudio* Windows2000/XP compatible.	96	Required for all first time users. Includes 1 year of technical support.
Caliente DLL	Dynamic link library (DLL) for the Delfin.	Requires ANSI-compliant C/C++ compiler. For example, Microsoft Visual C/C++. Windows2000/XP compatible.		Required for interfacing Host side code to DSP. May be used without Armada although not recommended
CCStudio C6000	Integrated development environment (IDE) for Target side development/debugging from Texas Instruments.	Requires XDS-510 compatible JTAG emulator for debugging capabilities.	89	Required for all first time users. Recommend use with Innovative Integration plug-n-play PCI JTAG emulator.
Armada	Host side development package using a revolutionary integrated development environment (IDE). Allows user to build/debug sophisticated data acq apps fully using MS Windows graphical environment quickly with Innovative Integration's Visual Component Libraries (VCL) of MFC Classes.	Requires Borland C++ Builder* or Microsoft Visual C++.	101	Recommended for inexperienced and seasoned C/C++ programmers. Offers easiest interface while providing the most flexibility and performance. Ties into a plethora of 3rd party components.

The Delfin Development Package contains all software packages listed above.

*Contact Innovative Integration for current release version.