

M6713

DSP/FPGA PCI Card with I/O Expansion

300MHz C6713 DSP (Floating Point)
User-configurable Spartan-3 FPGA
Off-the-shelf Analog I/O Cards
Open Architecture for Custom I/O
Dual FPDP external data ports

Features

- PCI 64-bit/66MHz
- Two I/O Expansion Sites
- Xilinx 1.5M gate Spartan3 FPGA
- I/O interface fully reconfigurable in FPGA
- FPDP Interface
- Extensive software support in source form
- Custom logic development supported for FPGA
- DSP/BIOS peripheral drivers
- Low cost

Applications

- PCI based real-time control
- High-end data capture & playback
- Industrial high-speed controls
- Test & Measurement
- Military equipment
- OEM instruments

Hardware Options

- DSP debugger
- I/O cables and terminal blocks



OMNIBUS Compatible

Analog and Digital I/O
Daughter Cards

Software Development Tools (included with purchase)

- C/C++ Dev Sys using TI Code Composer Studio
- Real-time OS: TI DSP/BIOS w/drivers for DSP periph
Device Drivers
- MS Visual C++ Host support
- Turnkey applications with source code
- C++ components for analysis, graphing, logging
- Tutorials

Ordering Information

M6713 with 1500k FPGA 80117-1



M6713

Overview

M6713 is a powerful and flexible DSP + FPGA board of novel architecture for advanced data capture and real-time control in PCI systems. The M6713 PCI card features a 300 MHz floating point DSP and 1.5M gate FPGA with an open IO architecture that is ideal for demanding applications in signal processing, controls and automation. As part of Innovative's modular family, Standalone and compact PCI version are also available with similar features. Supporting this open-architecture hardware platform, the Pismo software tool set provides target and host libraries, practical utilities and numerous example programs that illustrate the use of all board peripherals at full bandwidth and greatly accelerate end-user system development.

Processor Cores

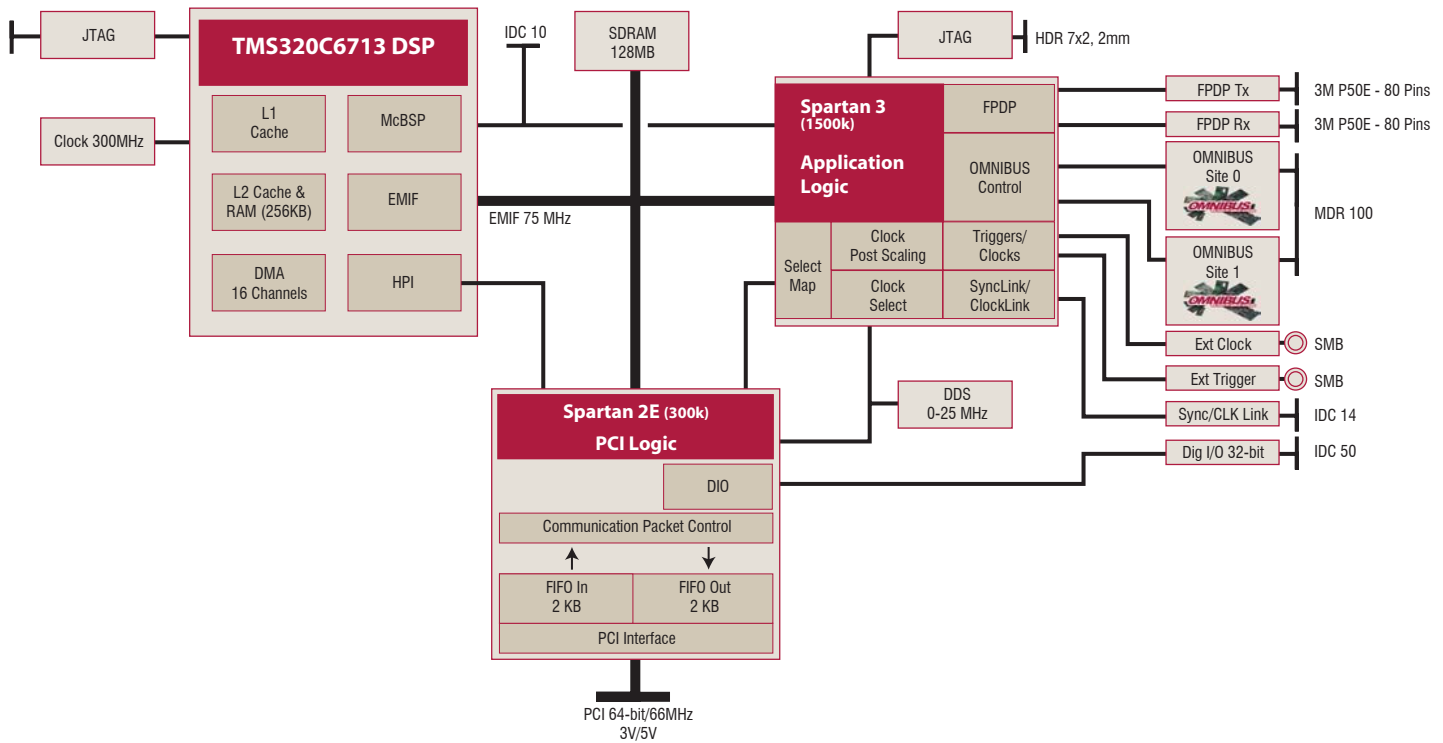
The M6713 is built around the powerful, C-friendly floating point TMS320C6713[®] DSP, that utilizes all strength and maturity of the C6000 series architecture. With 8 parallel execution units, 256KB of on-chip memory coupled with an efficient cache controller and 16 DMA channels, the C6713 offers unparalleled processing power and peripheral control in a user-friendly environment. The CPU clock is 300MHz while the 32-bit External Memory Interface (EMIF) bus is clocked at 75MHz.

The two-level cache controller uses an L1 cache of 4KB data and 4KB instructions, and 256KB that can be partitioned via software between L2 cache and unified mapped RAM. Additional memory is provided on the board with 64 MBytes of 1 wait-state synchronous SDRAM. The enhanced DMA controller handles 16 independent channels, which greatly relieves the CPU from bulk data movement and preserves its bandwidth for application-specific code. The EMIF is interfaced to a Xilinx Spartan-3 FPGA device for the Omnibus and IO control, and a Xilinx Spartan2E for PCI interface and control. Both McBSP sync serial ports are pinned out and interfaced to the logic.

Interrupt control is in the FPGA and allows control of edge/level source selection via software and DMA transfer count that supports interrupts for block movements.

The software libraries provided with the card make good use of DSP/BIOS peripheral drivers to facilitate end-user code development for the most complex multi-thread applications while optimizing bandwidth utilization. The toolset includes turn-key data acquisition and playback application with source code that illustrates the best utilization of all hardware resources. In particular, communicating with the host is simple with a powerful packet-based PCI transfer supporting both chained busmastering for high-speed data transfer as well as mailbox message for command and controls.

For applications requiring reconfigurable logic, either for integrating a custom external interface or for adding ultra-fast data processing, the Spartan-3 may be customized. The Spartan-3 family of FPGA provides a cost-effective logic fabric that incorporates multipliers, memory and logic cells for DSP and custom logic designs. The XC3S1500 featured on the M6713 provides 1,500K system gates, 576Kbits block RAM, 4 clock managers, 32 18x18 multipliers and ample I/O. The M6713 board exposes over 100 of these I/O pins to end user on the OMNIBUS connectors. The FrameWork Logic provided in source form, shows the OMNIBUS interface implementation as an example of a glue logic between IO mezzanine cards and the DSP EMIF bus. However, with the Spartan-3 device, possibilities are endless.



On Board Peripherals

The M6713 provides a complete set of peripherals to support all aspects of a typical integration in advanced systems, as illustrated in the functional block diagram:

- 64MB SDRAM memory
- Two I/O daughter card sites, Configured by default as OMNIBUS sites and Fully reconfigurable in FPGA
- Analog power supply to IO sites
- Two FPDP Ports (1 Transmit, 1 Receive) per VITA 17
- DDS Time Base 0-25MHz
- 32-bit DIO Port
- SyncLink/ClockLink for multi-card support
- 64bit/66MHz PCI interface, 3V or 5V
- Down-compatible with 32bit or 33MHz

I/O Daughter Card Sites with OMNIBUS support or custom configurable

M6713 offers two daughter cards sites for analog and digital I/O to be interfaced to the DSP EMIF bus. The interface implemented on the card as delivered is Innovative Integration's OMNIBUS, which supports a choice of 15+ off-the-shelf OMNIBUS modules that can simply plug-onto the M6713 to add the desired set of analog A/D or D/A channels or high-speed digital interface. From 32 simultaneous 200 kHz 16-bit A/D and D/A channels, to 65MSPS sampling for IF receive/transmit, to 100+ dB signal purity using 24-bit sigma-delta converters, the OMNIBUS family serves a very broad range of application, off-the shelf.

System integrators may also design custom OMNIBUS daughter card for installation on the M6713 to address very specific application requirements.

OMNIBUS is an open bus architecture that is flexible, easy to use and high-performance. It is a 37.5MHz synchronous parallel bus structure utilizing four decode (chip select) signals per site with 12-bit sub-addressing available. Module may be memory mapped into the DSP memory and drive multiple independent interrupt signals back to the DSP. Numerous timing, power and handshaking signals are provided. Full description of the specification is available in the Support section of our web site.

Finally, when a completely different interface is required, the Spartan-3 on the M6713 can be completely reconfigured by end-user. Innovative Integration then provides VHDL source of the OMNIBUS implementation with simulation test benches, which includes re-usable blocks such as constraint files and interface to the DSP EMIF bus. The connectors consist of a total of 100 pins -distributed over 4 connectors- that are direct connections to the FPGA DIO for each site, plus clean power supplies for +/-5V and +/-15V analogs, each capable of 500mA as well as 3.3V and 5V digital supplies.

FPDP External Data Ports

The Front Panel Data Port (FPDP) allows the transfer of data at high-speed and low latency between the M6713 and other hardware. There is one Transmit Master (TM) port and one Receive Master (RM) – or Receive (R) – port.

The M6713 FPDP ports conform to specification ANSI/VITA 17. It is designed for data streaming and provides basic support for flow control and framing. Each port is capable of 200MB/s, consisting in 32-bit parallel data port plus flow control signals and clock up to 50MHz. Data transfers are source synchronous, the TM generates a clock and uses this for output registers which drive the data bus. At the receiver, the same clock is used for input register which sample the data bus. A sync signal may be used to apply framing to data.

Receivers may assert a suspend signal to halt the data flow from the transmitter.

FIFO buffering is provided on the M6713 Receive port to allow for the response time of the transmitter to a suspend request.

FPDP signaling is straight forward, TTL compatible levels for all signals except the clock which is PECL. Configuration and utilization of the M6713 FPDP ports at maximum speed are well illustrated in software examples provided in the tool set.

System-Level Peripherals For Fast, Simple Integration

Digital IO Port - A simple high-speed memory-mapped, 32-bit latch is available to support general-purpose LVTTTL digital I/O, with ESD and overvoltage protection. Direction is software-configurable in bytes. The port may be software or externally clocked at rates to 20 MHz.

Accurate DDS Time Base - The output of an AD9851 digital synthesizer is routed to the logic, where post-scaling reduces jitter – for the 0–5MHz range – before presenting a very stable time base to both OMNIBUS sites. It provides a time base spanning 0 to 25 MHz programmable in increments of 0.01 Hz.

External Clock and External Interrupt input are available on SMB co-ax connectors with 50-ohm termination. Ext INT is used to trigger the execution of a particular processing routine on an external hardware event, while external clock signal is typically used to slave on-card analog conversion to an external time base.

Multi-card synchronization – The SyncLink/ClkLink interface allows up to four unique timing signals and event triggers to be shared between up to 16 cards. The M6713 card has a switch matrix that routes any event trigger to any SyncLink/ClkLink port, completely under software control. For instance, the DDS output can drive an LVDS pair to serve as external clock to other cards. There is no complex cabling, just a simple connection and software configuration.

User-Reconfigurable Logic

The M6713 is offered with user-reconfigurable logic — Spartan-3 device, 1.5 Million gates. The M6713 is supported by Innovative's FrameWork Logic system for customization. Custom logic can be developed in VHDL or MATLAB Simulink, providing a powerful environment that reduces development time for complex signal processing algorithms.

The FrameWork Logic for the M6713 logic includes hardware interfaces and control functions

that consume about 8% of the device, leaving ample resources for signal processing and new application features.

Further details of the logic development process are in the FrameWork Logic User Guide, online at Innovative's website. FPGA code development expertise, Xilinx ISE development tools and simulation tools are required for such development. Contact our sales department for details or engineering services.

Software Support

The M6713 Pismo tool kit is a powerful collection of software libraries, utilities, examples projects and interactive help file that allow developers to be very productive from the start. Numerous program examples – with source code– demonstrate the usage of every peripheral on the board as well as OMNIBUS expansion modules.

Pismo provides a framework for flexible and high-bandwidth communication with host PC systems at full PCI bandwidth, and offers handy utilities that simplify board utilization and truly accelerate system development such as simple boot methods, FPGA dynamic loading and DSP terminal emulator.

Target Side Tools - Extensive C/C++ libraries, example source code, DSP/BIOS peripheral drivers, mailbox messaging and bulk data transfer to/from PC are fully integrated in Texas Instruments' Code Composer Studio. Pismo makes extensive use of DSP/BIOS, TI's DSP operating system included in CCStudio, which simplifies code development of complex, multi-thread applications by providing drivers, scheduling services and run-time management of all DSP resources to optimize bandwidth. Users do not

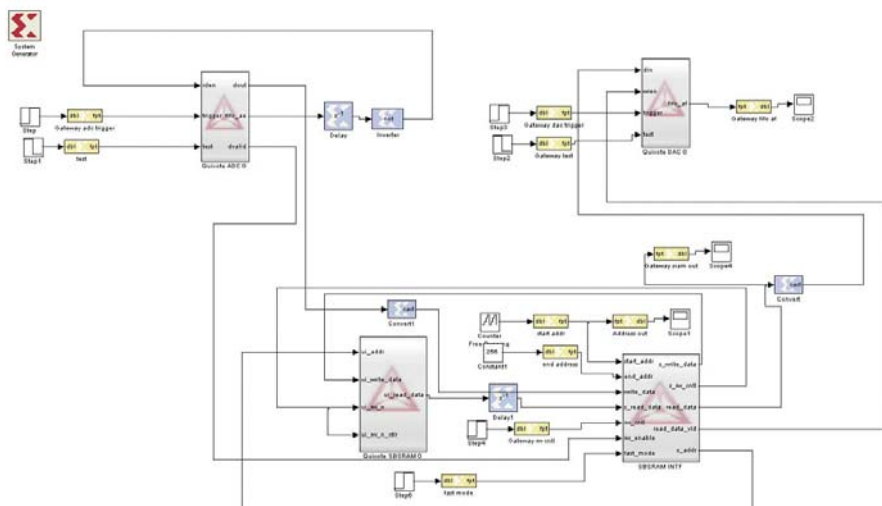
code to set up and control IO peripherals.

Another benefit of DSP/BIOS is a modular, easy to maintain code structure, way ahead of an old fashion, complex, main() program to structure task priorities and dependencies. At debug time, DSP/BIOS also provides real-time profiling to aid in optimizing code.

Host Side Tools – Pismo includes two groups of Host Side support tools: extensive C++ libraries –with sophisticated program examples- and turnkey utilities. Libraries include methods to control the M6713 (Reset DSP, Download code) and to communicate with the board via mailbox-style messages and bulk data transfer using busmastering. Both communication techniques are very intuitive and well illustrated in examples. Turnkey utilities – provided as executables – facilitate board utilization and program debugging at the beginning of a project. A simplified set-up for RTDX, the terminal interface provided with Code Composer Studio, and practical examples showing messages and data transfer between DSPs and CCStudio. BinView is a binary data viewer that graphs and analyzes data in time and frequency domain, and can be directly invoked from UniTerminal. These tools can co-exist at run-time with Code Composer Studio Debugger. The FPGA can be re-configured over the PCI bus with a utility that control SelectMap to stream a viable logic image directly to the device.

OEM Configurations

The M6713 board can be configured or modified to fit your specific requirements and provide an optimal mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.



A typical block diagram design using MATLAB

64-bit PCI DSP

Digital Signal Processor

300MHz Texas Instruments TMS320C6713 floating-point DSP
 L1 cache 4KB data/4KB program
 L2 cache + Unified RAM 256 KB
 Two multichannel buffered serial ports (McBSP)
 Two 32-bit timers
 Sixteen DMA channels
 32-bit external memory interface, clocked at 75MHz
 Two McBSP serial ports on external headers

Memory

64 MB SDRAM clocked at 75MHz

User-reconfigurable FPGA

Xilinx Spartan3 XC3S1500-4FG456C (1,500K gates, -4 speed grade is standard)
 Supports all I/O functions
 IO pins to FPGA :
 100 Omnibus connections
 79 FPDP connections
 33 DIO connections
 SelectMAP loading from PCI bus
 Example logic: Omnibus, FPDP, DSP bus
 Framework Logic
 VHDL source code with ModelSim test benches
 JTAG port for ChipScope and JTAG downloads

Clocks, Sync, Multi-card support

DDS 0-25MHz in 0.01Hz with post-scaling for low jitter
 Dual External SMBs (optional 50 ohm) for external clocks, triggers or interrupts input/output
 Synclink/Clocklink for sharing LVDS clock and TTL triggers
 Two High speed LVDS signal pairs for clocks
 Six TTL compatible signals for triggers.

Two OMNIBUS I/O sites

Independent clock and Interrupt support
 FPGA reconfigurable for custom IO interfaces
 Trigger support (Module dependent)
 Omnibus power supplied:
 +5V digital @ 1A, +5V analog @ 500 mA,
 -5V analog @ 500 mA, +/-15V analog @ 300 mA each, 3.3V digital @ 500 mA

Digital IO port

32 bidirectional bits, direction selected on a byte basis
 external clock input
 LVTTTL, direct from FPGA (0-3.3V signaling)
 5V tolerant
 Pulled up to 3.3V with 10K ohm resistors
 Each bit is ESD and over-range protected.

FPDP Ports

Conforms to VITA 17 spec
 One Tx, 32-bit data wide, 50MHz, 200MB/s
 One Rx, 32-bit data wide, 50MHz, 200MB/s
 2KB FIFO
 PECL or TTL clock (optional) transmission for 1-3 meter cable
 Supports fixed frame, single frame, variable length and single point data sync modes with frames up to 64KW long
 Interrupt on sync available
 May be used as digital IO (32 bit input on Rx, 32 bit out on Tx)

PCI Interface

64-bit, 66 MHz, 3V or 5V
 Down-selects to 32 bit and 33MHz if needed
 Packet mode interface:
 - Efficient packet transmission mechanism
 - Supports high rate continuous PCI data transfers
 80 MB/s on many 33 MHz, 32-bit platforms
 300 MB/s on many 66 MHz, 64-bit platforms
 - DMA interface to DSP with auto-pacing
 - Interrupts to DSP on packet transactions
 2KB FIFO in each direction
 HPI interface to DSP for code loading and communications
 Field-programmable, in-situ logic updating using supplied applet

Debug Ports

JTAG 1149.1 compliant emulation port for DSP
 Compatible with Innovative Code Hammer, TI XDS-510/560 compliant debugger
 JTAG for FPGA (compatible with Xilinx cables such as Parallel Cable IV)

Connectors

SMB, Ext Clocks (2)
 MDR-100, Omnibus external signals (50 pins per site)
 AMP-173280, 50pin, Omnibus sites on-board with
 100+ pins straight-connect to FPGA DIO
 3M P50E 80pin, FPDP Tx and Rx ports
 IDC-50 polarized male, Digital IO
 IDC-14 polarized male, DSP JTAG
 IDC-14 polarized male, Synclink/ClockLink
 IDC-10 polarized male, FPGA JTAG
 2x5 header, McBSP's

Size

1/2 Size PCI (short card)
 64-bit 3V/5V connector

Power

4 W typical
 5V, +12V, -12V supply from PCI bus
 +/-12V only required when +/-5V analog power to Omnibus is needed

Operating Conditions

10-55 degrees C
 Some configurations may require forced air

Development Languages

DSP: C++ under Code Composer Studio, MatLab/Simulink for modelling and code generation
 Pismo Toolset includes libraries, projects, utilities, help files
 Host PC: MS Visual C++, .NET, Borland C++ Builder,
 Framework Logic in VHDL supported by
 Logic : VHDL with Xilinx ISE, Mentor Graphics ModelSim, MatLab and Xilinx System Generator

Accessories

Analog and Digital I/O : See Omnibus Modules
 MDR100 Cable and Breakout for Omnibus IO 80051-1
 SMB to BNC cable, 1M 67021

Documentation for M6713

M6713 Hardware user Guide
 Framework Logic User Guide
 Malibu Software Deveolpment Manual



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