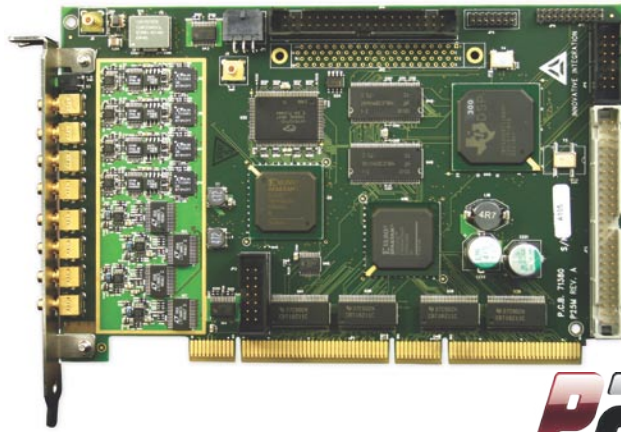


# P25M

## DSP/FPGA PCI Card with Analog I/O

300MHz C6713 DSP (Floating Point)  
User-configurable Spartan-3 FPGA  
Four 25MSPS • 16-bit A/D  
Four 50MSPS • 16-bit D/A



# P25M

### Features

- PCI 64-bit/66MHz
- >85 db SFDR analog IO
- Xilinx 1M gate Spartan3 FPGA
- 65 bits digital IO
- DSP Memory: 128MB DRAM
- FPGA Memory: 2MB SRAM
- Extensive software support in source form
- Custom logic development supported for FPGA
- DSP/BIOS peripheral drivers

### Applications

- PCI based real-time control
- High-end data capture & playback
- Industrial high-speed controls
- Stimulus- response measurements
- OEM instruments

### Hardware Options

- DSP debugger
- I/O cables

### Software Development Tools

- C/C++ Dev Sys using TI Code Composer Studio
- Real-time OS: TI DSP/BIOS w/drivers for DSP periph
- MS Visual C++ Host support
- Turnkey applications with source code
- C++ components for analysis, graphing, logging
- MATLAB and VHDL FrameWork Logic Dev Tools

### Ordering Information

P25M	80169-0
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### Overview

P25M is a powerful and flexible DSP + FPGA for signal processing and real-time control in PCI systems. The P25M PCI card features a 300 MHz floating point DSP and 1M gate FPGA with 4 channels of 25MSPS, 16-bit A/D and 4 channels of 50MSPS, 16-bit D/A. Supporting this open-architecture hardware platform, the Pismo software tool set provides target and host libraries, practical utilities and numerous example programs that illustrate the use of all board peripherals. The FrameWork Logic development tools provide comprehensive support for adding signal processing to the FPGA. The full-featured logic and DSP programming tools greatly accelerate all facets of the system development.

### DSP Core

The P25M is built around the powerful, C-friendly floating point Texas Instruments TMS320C6713<sup>®</sup> DSP. The '6713 has 256KB of on-chip memory coupled with an efficient cache controller. The CPU clock is 300MHz while the 32-bit External Memory Interface (EMIF) bus is clocked at 75MHz.

The P25M main memory is 128MBytes of synchronous SDRAM clocked at 75MHz. The enhanced DMA controller handles 16 independent channels, which assists the CPU with data movement and preserves its bandwidth for application-specific code. Both McBSP sync serial ports are pinned out to connectors.

The DSP is programmed using Texas Instruments DSP/BIOS, a high performance DSP RTOS. The software libraries provided with the card include DSP/BIOS peripheral drivers for all peripherals. The toolset includes turn-key data acquisition and playback application with source code that illustrates the best utilization of all hardware resources. In particular, communicating with the host is simple with a powerful packet-based PCI transfer supporting both chained busmastering for high-speed data transfer as well as mailbox message for command and controls.

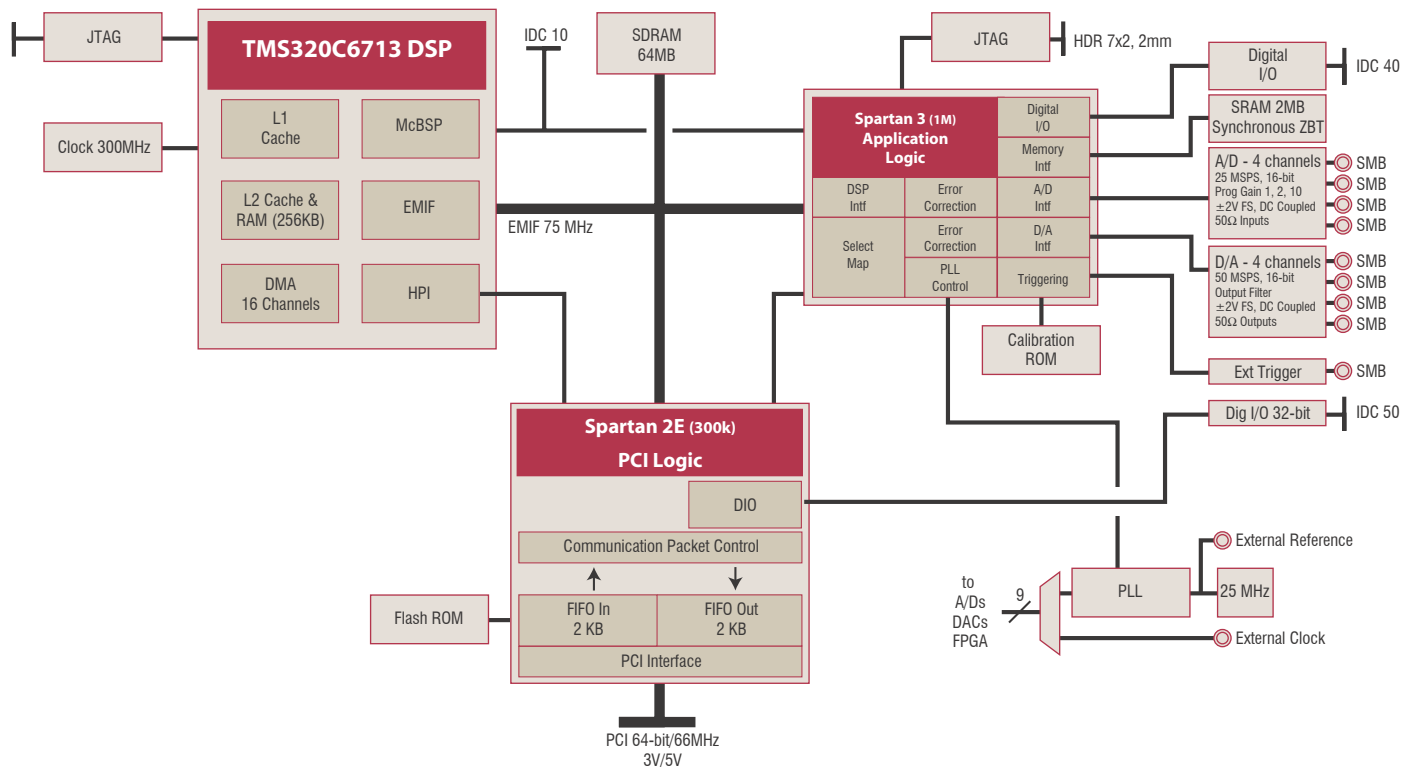
### FPGA Core

The FPGA logic is reconfigurable on the P25M and may be customized using the FrameWork Logic development tools. The Xilinx XC3S1000 FPGA featured on the P25M provides 1M system gates, multipliers and embedded memory blocks. The P25M exposes over 33 of these I/O pins to end user on the digital I/O. The FPGA has 2MB SRAM memory, useful for computational or buffer memory.

The FrameWork Logic for the P25M supports VHDL and MATLAB development tools for IP development. The logic is configured from the PCI host through select MAP. The standard logic consumes about 20% of the logic. Further details of the logic development process are in the FrameWork Logic User Guide, online at Innovative's website.

### Analog I/O

The P25M integrates 4 A/D and 4 D/A channels with the FPGA core. The channels are independent, simultaneously sampling with >90dB dynamic range - ideal for stimulus response measurements and servo applications. The A/Ds and D/As have a direct connection to the FPGA for high-speed DSP applications in the FPGA.



The A/Ds and D/As may be clocked externally or from a low jitter PLL. Triggering features in the FPGA include framed capture, external or software triggers.

All analog I/O is 100% calibrated on each card. Digital error correction in the logic is provided and uses an on-card non-volatile memory for calibration coefficients

### System-Level Peripherals For Fast, Simple Integration

**Digital IO Ports** - Port 1: 32 bits implemented as memory-mapped, 32-bit latch for general-purpose LVTTTL digital I/O, with ESD and overvoltage protection. Direction is software-configurable in bytes. The port may be software or externally clocked at rates to 40 MHz. Port 2: 33 bits direct to FPGA.

**Accurate PLL Time Base** - An AD9510 PLL and clock distribution device provides a low-jitter, stable clock that may be used as a sample clock. The PLL outputs have a range of 4.765 MHz to 50 MHz with a 150 MHz / N (N=1..32) resolution.

External Clock and External Interrupt input are available on SMB co-ax connectors with 50-ohm termination. Ext INT is used to trigger the execution of a particular processing routine on an external hardware event, while external clock signal is typically used to slave on-card analog conversion to an external time base.

### Software Support

The P25M Pismo tool kit is a powerful collection of software libraries, utilities, examples projects and interactive help file that allow developers to be very productive from the start. Numerous program examples - with source code- demonstrate the usage every peripheral on the board.

**Target Side Tools** - Extensive C/C++ libraries, example source code, DSP/BIOS peripheral drivers, mailbox messaging and bulk data transfer to/from PC are fully integrated in Texas Instruments' Code Composer Studio. Pismo makes extensive use of DSP/BIOS, TI's DSP operating system included in CCStudio, which simplifies code development of complex, multi-thread applications by providing drivers, scheduling services and run-time management of all DSP resources to optimize bandwidth. Users do not need to understand hardware-specific low-level code to set up and control IO peripherals.

**Host Side Tools** - Pismo includes two groups of Host Side support tools: extensive C++ libraries -with sophisticated program examples- and turnkey utilities. Libraries include methods to control the P25M (Reset DSP, Download code) and to communicate with the board via mailbox-style messages and bulk data transfers. Turnkey utilities - provided as executables - provide logic and DSP loading and assist with program debugging at the beginning of a project. A simplified set-up for RTDX terminal in-

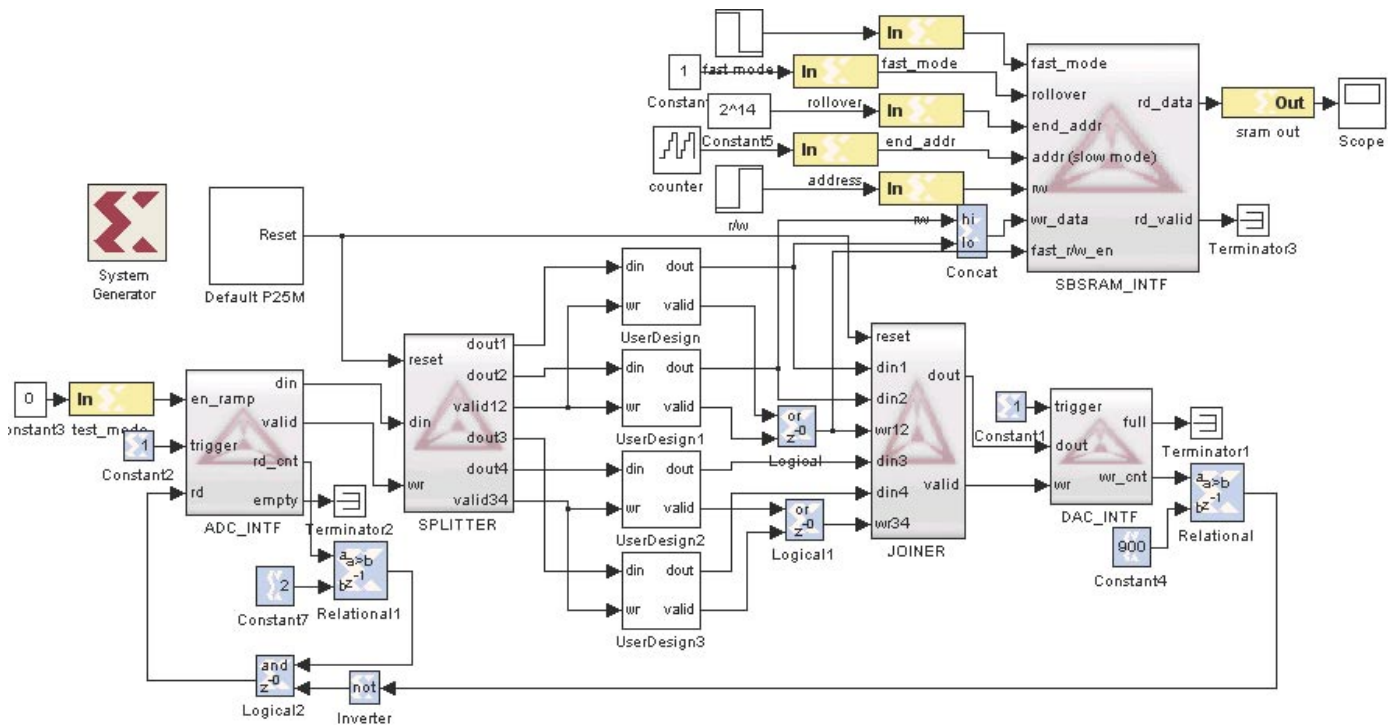
interfaces provided for Code Composer Studio, and practical examples showing messages and data transfer between DSPs and CCStudio. Additional provided tools for data viewing (BinView) and target communications (UniTerminal) can be used with Code Composer Studio Debugger to aid in DSP application development.

## FPGA Logic Development

Logic development using VHDL and MATLAB is supported. The FrameWork Logic User's Guide fully describes the VHDL logic, which includes peripheral interfaces for all analog I/O and the DSP.

The VHDL FrameWork Logic is used as a hardware interface layer that can be modified to include new IP cores and add unique features such as signal processing and triggering. The logic components for each hardware interface provide a simple data stream interface that is used to add new functionality to the design either in VHDL, IP cores from MATLAB, or third party IP cores. Complete source code, constraints and Xilinx ISE project files are provided.

The board support package for MATLAB SimuLink and Xilinx System Generator provides a comprehensive development and simulation toolset for DSP development and testing.



Block sets for the P25M include A/D, DAC, DSP and memory interfaces that provide full hardware access to MATLAB users.

The P25M board support library is integrated with MATLAB and Xilinx System Generator providing full access to the P25M peripherals and DSP. Gateways between MATLAB and the hardware allow hardware-in-the-loop testing for IP development and verification. Examples illustrate the use of the analog IO, memory and DSP interface from within the MATLAB environment. When the development in MATLAB is complete, the logic is easily integrated with the FrameWork Logic for fully embedded operation by including the IP core into the VHDL project and compiling the system.

## OEM Configurations

The P25M board can be configured or modified to fit your specific requirements and provide an optimal mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.

## Digital Signal Processor

300MHz Texas Instruments TMS320C6713 DSP  
 32-bit floating-point  
 L1 cache 4KB data/4KB program  
 L2 cache + Unified RAM 256 KB  
 Two multichannel buffered serial ports (McBSP)  
 Two 32-bit timers  
 Sixteen DMA channels  
 32-bit external memory interface, clocked at 75MHz  
 Two McBSP serial ports on external headers

## Memory

128 MB SDRAM clocked at 75MHz  
 16 kbit serial EEPROM (used for calibration)

## User-reconfigurable FPGA

Xilinx Spartan3 XC3S1000-4FG456C (1,000K gates, -4 speed grade is standard)  
 Supports all I/O functions  
 IO pins to FPGA : 33 DIO connections  
 SelectMAP loading from PCI bus  
 MATLAB Simulink Board Support Package  
 Framework Logic provides standard functionality  
 VHDL source code with ModelSim test benches  
 JTAG port for ChipScope and JTAG downloads

## Clocks and Triggering

PLL with post-scaling for Low jitter: <1ps RMS  
 4.68MHz to 50 MHz  
 Dual External SMBs (optional 50 ohm) for external clocks, triggers or interrupts input/output  
 External, software and framed trigger modes

## Digital IO ports

### Port 1

32 bidirectional bits, direction selected on a byte basis  
 external clock input  
 LVTTTL, direct from FPGA (0-3.3V signaling)  
 5V tolerant

### Port 2

32 bidirectional bits, direction selected on a byte basis  
 external clock input  
 LVTTTL, (0-3.3V signaling)  
 5V tolerant  
 ESD and overrange protection



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## A/D Channels

Channels	4 Independent
Sample Rate	1 to 25 MSPS
Resolution	16-bit
Input	±2V, DC Coupled
Input Impedance	50ohm
Program. Gain	1, 2, 10
Analog In Bandwidth	-3dB @ 12 MHz
A/D Devices	LTC2203

## DC Specifications

Offset Error	Calibrated to <1mV
Gain Error	Calibrated to <0.05%fs
Linearity Error	<1.5 LSB

## AC Specifications

SFDR	>88 dB, 100kHz, 5 MSPS
ENOB	>11.7 bits, 100kHz, 5 MSPS
S/N	>90 dB, 100kHz, 5 MSPS

## D/A Channels

Channels	4 Independent
Sample Rate	0 to 50 MSPS
Resolution	16-bit
Input	±2V, DC Coupled
Input Impedance	50ohm
Output Bandwidth	-3dB @ 12MHz
DAC Devices	LTC1668

## DC Specifications

Offset Error	Calibrated to <1mV
Gain Error	Calibrated to <0.05%fs
Linearity Error	<±4 LSB typ

## AC Specifications

SFDR	84 dB, 14kHz, 25 MSPS update
ENOB	11.7, 14kHz, 25 MSPS update
S/N	82 dB, 14kHz, 25 MSPS update
Glitch Impulse	<1mV peak, <5ns

## PCI Interface

64-bit, 66 MHz, 3V or 5V  
 Down-selects to 32 bit and 33MHz if needed  
 Packet mode interface:

- Efficient packet transmission mechanism
- Supports high rate continuous PCI data transfers
  - 80 MB/s on many 33 MHz, 32-bit platforms
  - 350 MB/s on many 66 MHz, 64-bit platforms
- DMA interface to DSP with auto-pacing
- Interrupts to DSP on packet transactions

HPI interface to DSP for code loading and communications  
 Field-programmable, in-situ logic updating using supplied applet

## Debug Ports

JTAG 1149.1 compliant emulation port for DSP  
 Compatible with Innovative Code Hammer, TI XDS-510/560 compliant debugger  
 JTAG for FPGA (compatible with Xilinx cables such as Parallel Cable IV and platform USB)

## Connectors

SMB: Ext Clocks (2), A/D inputs (4), D/A outputs (4)  
 IDC-50 polarized male, Digital IO  
 IDC-14 polarized male, DSP JTAG  
 IDC-40 polarized male, FPGA Digital I/O  
 IDC-10 polarized male, FPGA JTAG  
 2x5 header, McBSP's

## Physical Data

1/2 Size PCI (short card)  
 64-bit 3V/5V connector  
 Weight: 160 grams

## Power

4 W typical (varies with DSP & FPGA application)  
 3.3V, 5V supply from PCI bus

## Operating Conditions

0-70 degrees C (noncondensing)  
 Some configurations may require forced air  
 Designed to meet ETS 300 019-1.1 Class 1.2, ETS 300 019-1.2 Class 2.3, ETS 300 019-1.3 Class 3.3

## Development Languages

DSP: C++ under Code Composer Studio, MATLAB/Simulink for modelling and code generation  
 Pismo Toolset includes libraries, projects, utilities, help files  
 Host PC: MS Visual C++, .NET, Borland C++ Builder,  
 Logic : VHDL with Xilinx ISE, Mentor Graphics ModelSim, MATLAB and Xilinx System Generator

## Accessories

SMB to BNC cable, 1M 67021

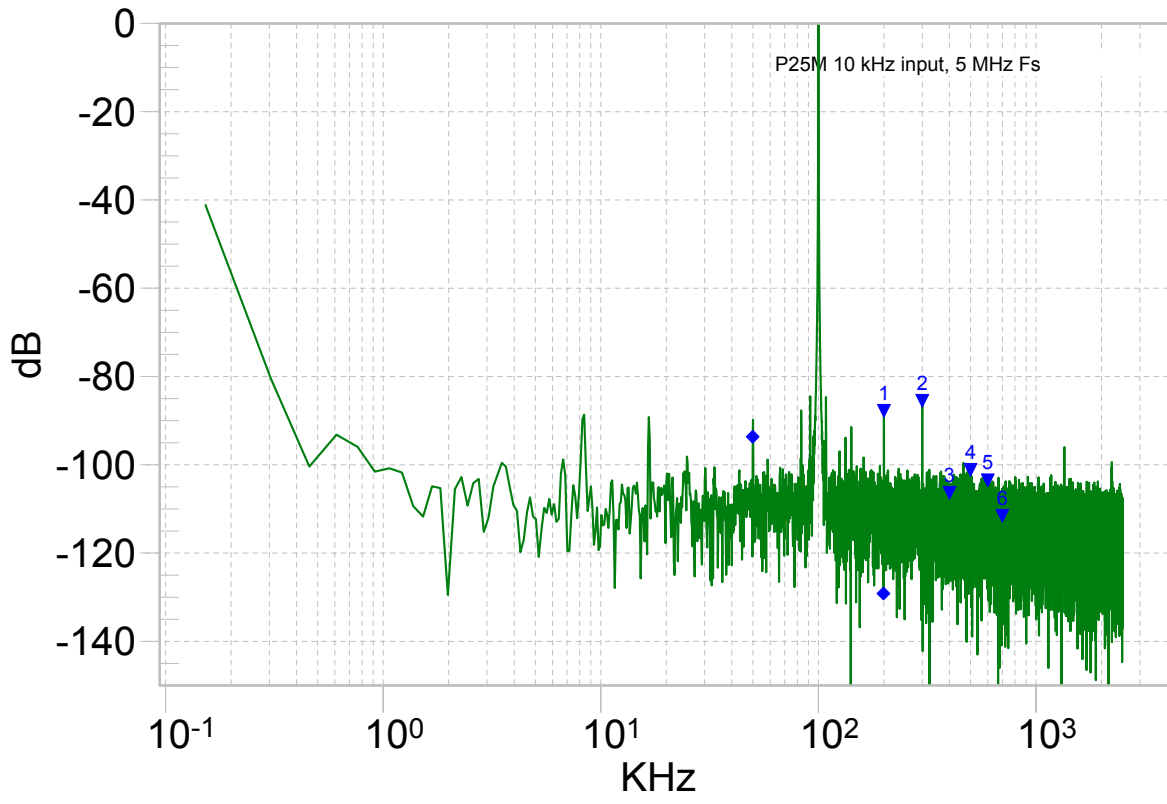
## Documentation for P25M

P25M Hardware user Guide  
 FrameWork Logic User Guide  
 Malibu Software Development Manual

## Environmental Data

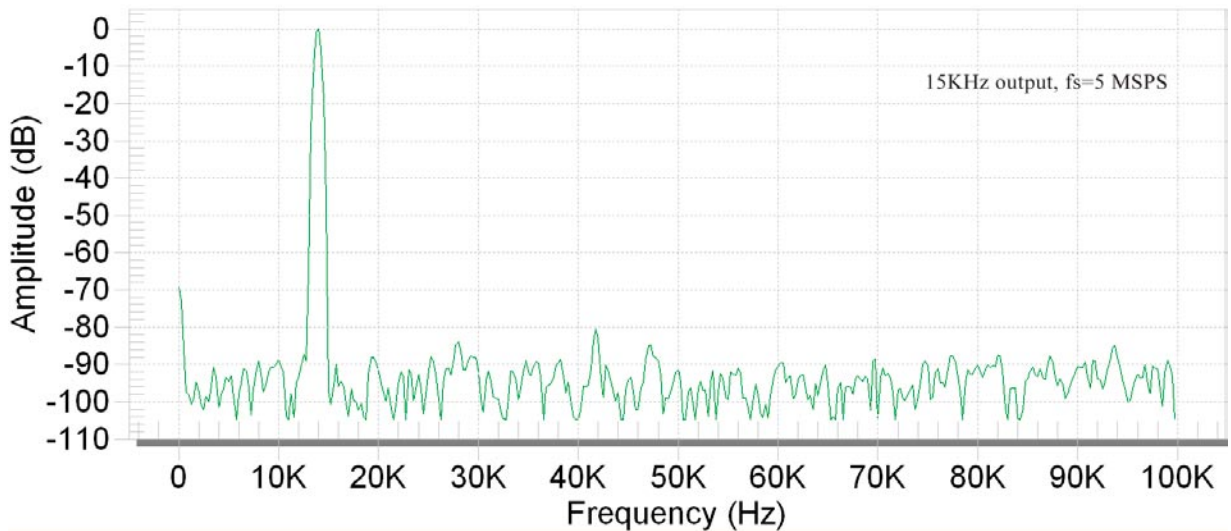
Lead Free  
 ROHS Compliant

# Frequency Response



Max S/N (dB)	S/N (dB)	SINAD (dB)	ENOB	SFDR (dB)	THD (%/dB)
98.1	74.9	72.4	11.7	88.7	0.006051 (84.4dB)

# DAC Output Spectrum



S/N: 81.4 dB	SINAD: 71.1 dB	SFDR: 84.1 dB
Max S/N: 98.1 dB	Enob: 11.5 bits	THD: 0.0194 % (74.2 dB)