

Quadia

DSP+FPGA Card

Four C6416 DSPs up to 1GHz each
Two Virtex-II Pro FPGAs, 4 M gates
Two PMC/XMC Sites tied to FPGA
Dedicated High-Performance Data Plane

Features

TMS320C6416 DSP (x4) up to 1GHz
32MB SDRAM per Processor
Two XC2VP40 VirtexII-Pro 4M gates
1.2 GB/s Data Plane
64-bit/133MHz PCI/PCI-X
Two PMC/XMC Sites with P4 pinned to FPGA
Dual Serial FPDP Data Port to 2.5 Gbps
Integration with PICMG 2.16 Ethernet Systems Support
Up to two 2MB private SBSRAM per FPGA
Up to two 32MB private DDR SDRAM per FPGA
64MB Global DDR SDRAM

Applications

High -End Co-Processing
Wireless, Broadband Communications
Signal Intelligence, Electronic Warfare
RADAR
Video
Biometrics

Hardware Options

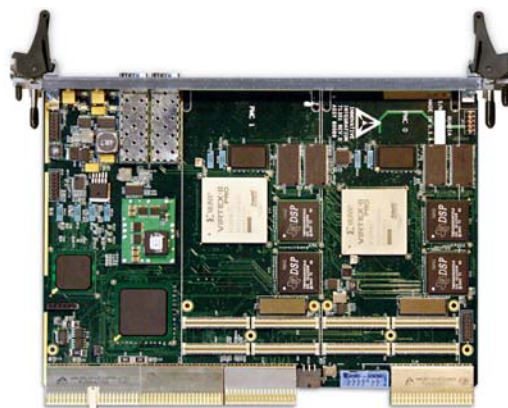
CodeHammer Debugger

Software Development Tools

Pismo Toolset
TI Code Composer Studio
MATLAB SimuLink for FPGA
VHDL Source Code & Test Benches

Ordering Information

Quadia no FPGA/RAM	80089-0
Quadia Two 4M FPGA & RAM	80089-2
Dual DSP available	
XC2VP50 FPGA 5M gates available	



Quadia

Overview

Quadia, a quad-DSP, dual FPGA, dual PMC/XMC site, CompactPCI board with advanced architecture providing unprecedented processing and IO connectivity, delivers blazing performance with extreme flexibility for advanced signal capture and real-time processing applications. MATLAB and TI DSP tools provide an advanced environment for signal processing that significantly shortens application development time.

The board features four TMS320C6416 DSPs, two Virtex-II Pro FPGAs and two PMC/XMC sites, connected with both a dedicated, high performance data plane and a flexible PCI bus architecture. Demanding real-time applications such as wireless communications, RADAR and signal intelligence can integrate high speed IO with signal processing in FPGAs and TI DSPs.

Quadia is supported by powerful DSP software and FPGA firmware design tools that reduce application development time. TI's Code Composer Studio, DSP BIOS plus Innovative's Malibu Toolset provide DSP programmers with a design tools and software that is full-featured and productive. FPGA firmware development using Quadia's Framework Logic allows signal processing designs to be developed directly in MATLAB or VHDL and directly implemented in firmware.

Main Features and Architectural Benefits

Quadia integrates power signal processing DSPs and FPGAs with IO using a dedicated data plane and a PCI bus architecture.

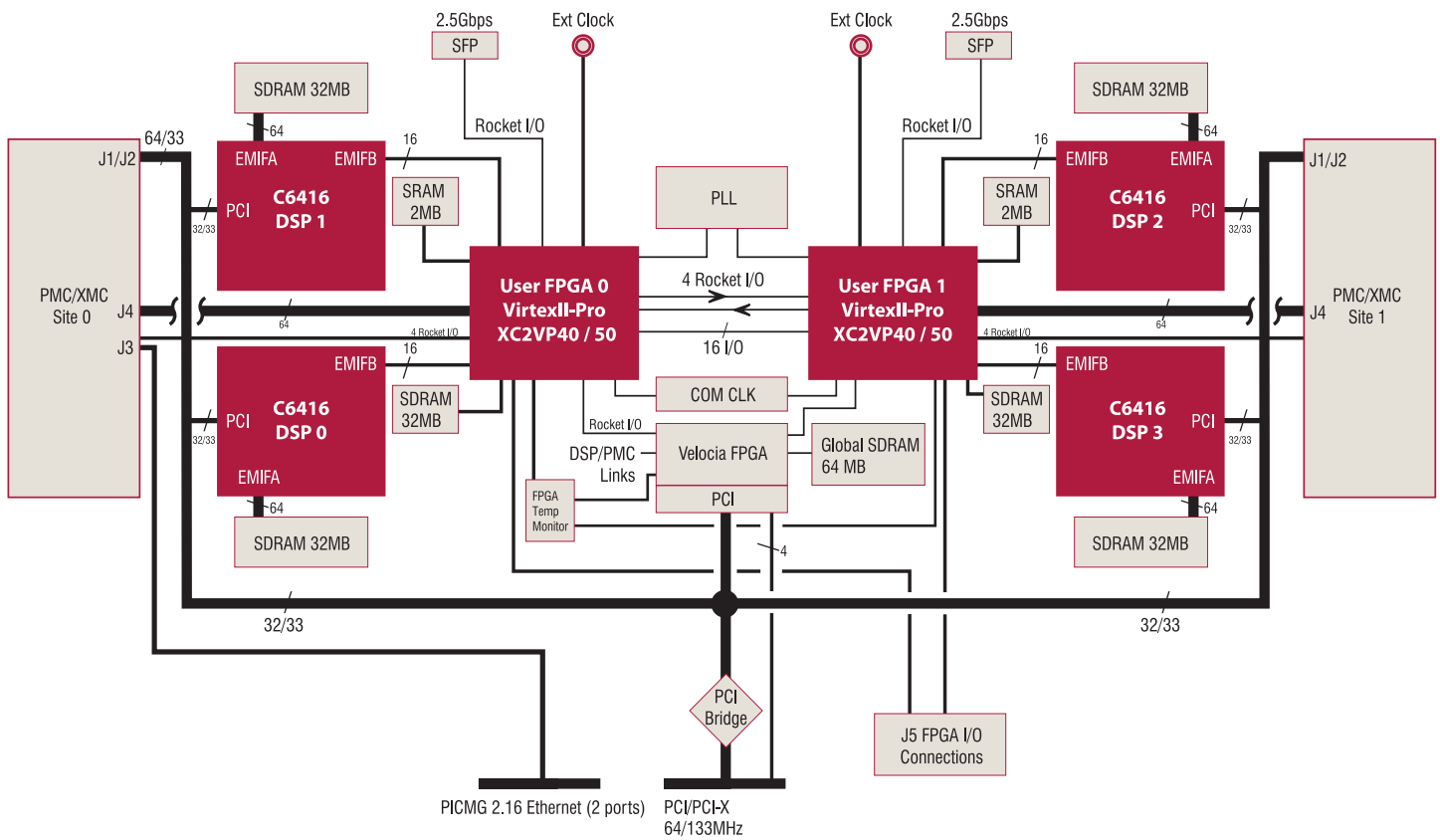
- Four 1 GHz, TI 'C6416 DSP cores with 64 MB memory each
- Dual Xilinx Virtex2 Pro VP40/50 FPGAs with local memory
- Dedicated data plane integrating the DSPs, FPGAs, PMC IO, and external devices with multiple, simultaneous 200 MB/s paths
- Flexible local PCI bus integrating the DSPs, PMCs, local memory pool & host interface controls.
- 2.5 Gbps capable external copper or optical IO ports
- Dual PMC/XMC sites for standard IO expansion. XMC provides up to 8 Gbps connectivity from XMC to Quadia FPGA.
- Rear terminal expansion interface to each FPGA
- Timing and system control features for IO and system integration.

Two Ethernet ports are pinned on PMC site) per PICMG 2.15 and routed to the backplane connector per PICMG 2.16.

Powerful TI DSPs

Quadia features four Texas Instruments' TMS320C6416 1GHz processors, the industry fastest 32-bit DSP chip, for 32,000 MIPS of aggregate power. The C64x DSP, a member of TI's C6000 family, is software compatible with TI's C62x, facilitating migration from C62x design. On chip RAM consists of a 2-level cache with 128Kbits of L1 program Cache, 128Kbits of L1 Data Cache and 8Mbits of L2 Unified RAM/Cache that can be partitioned by user via software. This cache structure makes external memory usage about 85% as efficient as on-chip memory. Other on-chip resources include a 32-bit PCI interface, 64 enhanced DMA channels, 3 timers and the HPI port. Each DSP is fitted with a private 32 MB of external





133MHz SDRAM, mapped on the 64-bit EMIFA bus. This wide bus is best used for private memory use in order to optimize tasks running on a given processor, as is often the case for block-oriented data processing. The built-in PCI core allows for flexible, user-friendly communication between the DSP, the host and any other device mapped on the bus. The 16-bit EMIF-B external interfaces are 133MHz and are connected straight to their local user-FPGA for inter-processor communication.

The two user-FPGAs are XC2VP40 Virtex-II Pro devices of Xilinx's high-end family of "platform FPGAs." The VP40 chip provides over 46K logic cells, 3.4Kb of Block RAM, 192 dedicated 18x18 multipliers, 8 Digital Clock Managers and over 800 user I/O, as well as 2 PowerPC processor cores and 12 RocketIO transceivers. These assets are utilized in Quadia's integration and leave ample resources for end-user code for a flexible integration of the most demanding signal processing algorithms such as down/up conversion, complex filtering, resampling, spreading/despreading and real-time signal analysis. For example, the Xilinx DDC core for GSM consumes only 1373 slices (< 10K gates) and 1 multiplier.

These FPGAs are almost 100% available for end-user code and represent enormous resources. A VP50 is pin-compatible and can also be offered as option. The FPGA ties the 16-bit 133MHz EMIF-B bus as well as the McBSP serial ports of each DSP, the P4- 64 pins connector of the PMC site and 8 other pins of P3. Four Rocket IO links to the XMC modules provide up to 10 Gbps connectivity to IO modules. This link can provide a data pipe bandwidth of up to an 800MB/s between logic, daughter and external hardware with off-the-shelf or custom PMC card. These cards can be connected to this huge engine for ultra fast, hardware-assisted processing. Firmware can be configured dynamically via SelectMap controlled by the central FPGA. As for memory, each user-FPGA has two banks of private memory: 2MB of fast SBSRAM and 32MB of DDR SDRAM. This dual type memory scheme is simply the best design for performance and flexibility: the SBSRAM provides a simple control and linear memory model that is fast and very easy to use while the SDRAM provides ample storage for very large sets of data or instructions

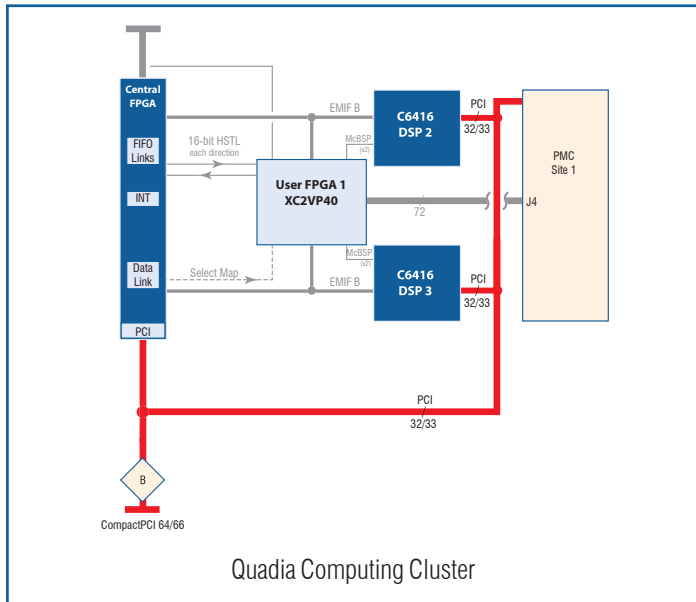
Superior Inter-Processor and External Communication Network

The main innovations of the Quadia architecture reside in the unmatched connectivity between DSPs, FPGAs, host and external hardware. In all multi-processor applications, the most crucial aspect that leverages overall performance is the intra- and inter-processor communication efficiency, both in terms of latency and bulk data transfer bandwidth. Utmost attention was given to this aspect early on in our design and the resulting multi-path scheme will satisfy the most demanding applications. Optimal connectivity between DSPs is provided with two separate communication planes:

- PCI-bus system, which can be thought of as the control plane, expandable, user-friendly
- Dedicated, private data plane built on Rocket IO links between FPGAs and XMC sites and DSP EMIF B connections extensible using the SFP Ports.

Control Plane using PCI bridged busses: Open Architecture and User-friendly

Quadra is a PCI-X device with hot-swap capability. The PCI bus provides a strong platform, well accepted for its bandwidth, user-friendliness and system integration capability. Quadra has a PCI bus bridge from the Host that implements a 33 MHz, 64 bit local bus. The local bus integrates the DSPs, PMC modules (64-bit), and memory pool. The DSP can communicate directly with the host over its PCI interface for system integration and control. All local PCI devices enumerate in the system and are visible by the system drivers. The DSP code loading, FPGA loading, card controls and PMC configuration are performed using the PCI bus interface.



The Velocita FPGA provides a large Global Memory pool of 64MB DDR SDRAM. Quadra may also busmaster to any PCI address, as commanded by any DSP or PMC module (module specific). This allows complete flexibility in system design and integration using the PCI bus

Quadra uses a transparent PCI bridge to allow the host processor to communicate with any PCI device on Quadra as a native device. Each device (DSP, PMC module, or global memory pool) can be accessed by any other device over the PCI bus. The host system is responsible for enumeration and resource allocation. Quadra is PICMG 2.1 compliant.

IO Expansion

The PMC (PCI Mezzanine Card) form factor is a well accepted standard that provides a performance-oriented expansion site. Many offerings of mezzanine cards with specialized I/O are available in this configuration. The first obvious utilization of these sites is the integration of high-speed analog I/O channels, Ethernet connectivity, or PowerPC co-processing power. Innovative Integration offers a family of PMC/XMC modules for wideband and narrowband digital receivers, acoustic channels and high-speed digital I/O applications. Custom design interfaces can also be quickly implemented, using legacy hardware or completely new designs.

Quadra integrates into PICMG 2.16 Ethernet backplanes, with two Ethernet ports pinned on PMC site 1, P4 connector, and direct path to the back plane connectors and provides a signal processing solution for base station and

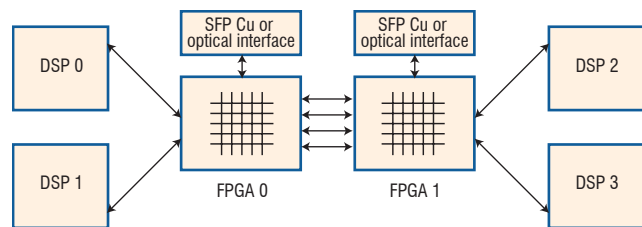
communication systems. Off-the-shelf PMC Ethernet cards are available off the shelf with GPP processors that easily provide the high-level communication layers.

Data plane provides communication mesh using simple packet based protocol

Quadra also implements a separate data plane for ultra-fast, low latency data transfer between devices, clusters and external hardware. Sustained data rates of up to 2 Gbps (200MB/s) are supported. A powerful and user-friendly communication scheme is implemented in the two Virtex-II Pro FPGAs with a link supporting each DSP, external IO through SFP ports and four links between FPGAs. The scheme uses a connection mesh that provides a private data path to and from each DSP. This may be easily modified in custom logic designs to support new topologies with arbitration. The software layer utilizes the DSP DMA channels for all data movement over the EMIF busses in order to preserve CPU bandwidth.

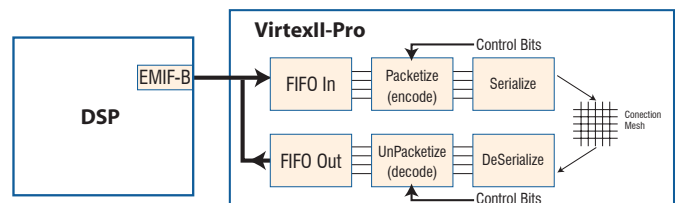
The data plane in each FPGA maps all 8 devices, namely:

- The four DSPs EMIF-B busses
- The two application FPGAs
- Two high-speed serial ports (one on each FPGA)



Concurrent paths are supported through the connection mesh, allowing many DSPs to transfer simultaneously.

The data plane is simple and easy to use. Each port manages data flow using



one DMA channel per direction so that any DSP can send data to any other DSP or external serial port with a single command to initiate DMA transfer. Each port is connected to the DSP 16-bit data bus and supports data writes to the FIFO at full rate - 16 bit at 133MHZ. Data is paced by available space in the data path FIFOs.

Flexible System Expansion

Communication with host system and external hardware is multifaceted, user-friendly and scalable. The peripheral list speaks for itself:

- Host PCI-X interface 64bit/ 133MHz, hot-swappable
- XMC/PMC sites 64bit/33MHz
- PCI and 4 lanes of 2 Gbps serial data
- PMC P4 connector directly pinned to FPGA Digital IO (72 pins total each)
- Ethernet ports (not PHY) pinned from 2.16 backplane to PMC, per PICMG 2.15 (Supports Ethernet processor PMC cards)
- Two SFP connectors from FPGA, capable of 2.5 Gbps full duplex
- J5 cPCI connector provides direct connections to both VP40 FPGAs

Each Virtex-II presents an external link interface in the shape of a Small Form Factor (SFP) connector. These SFP connectors support ultra-fast serial communication over copper or fiber, and many standard modules and links are available off-the-shelf. The logic framework delivered with Quadia implements a FIFO to Rocket IO connection which support bi-directional transfers at 2.5Gbps.

The SFP ports provide a convenient and standard high speed serial data stream that may transmit over extended distances over copper or fiber optic cable, and has great flexibility in supporting various topologies. The interface on each end of the link is a simple FIFO interface that is easily integrated into logic or DSP designs. All Rocket IO specific controls, including flow control across the link, are integrated into the standard Framework Logic components. These may be used "out of the box" without learning and debugging high speed Rocket IO links.

Development Tools

Quadia is delivered with the Pismo Toolset, a full suite of software development tools working under TI's Code Composer Studio. The Pismo Toolset makes DSP development fast and simple, with a complete collection of target and host side libraries and very illustrative and performance code example. It includes everything from convenient utility applets allowing reset, download, execution and high level debugging of DSP applications, to a complete set of source code examples demonstrating full operation of all the board features, including inter-processor communication, external port operation at full bandwidth as well as PCI busmaster and mailbox messaging.

The Pismo Toolset is fully integrated in Texas Instruments' Code Composer Studio and comes with CCS project and configuration files. Pismo supports and extends each of the features of DSP/BIOS on the Quadia board through a seamless integration of advanced C++ class libraries, BIOS-compliant DSP peripheral device drivers, and clear, illustrative examples. The device drivers fully exploit the available DMA channels in the C64x chip so that hardware interrupt rates remain low and preserve CPU bandwidth.

Host side development tools offer the most powerful and flexible means to rapidly integrate real time signal processing into Windows applications. They include powerful C++ classes that greatly facilitate the control of- and the communication with- the DSP targets from a host application, such as booting, downloading of code, message exchange via mailboxes and bulk data transfer via busmastering. These functions are easily called and configured from within Microsoft Visual C++ or Borland C++ Builder and shields the user from having to fully understand the inner details of the device-driver and hardware, though source code is available to end-user.

Debugging

Hardware and source-level debug operation is supported with Texas Instruments' Standard JTAG emulator compliant with XDS510 or XDS560, using a four-processor scan path.

Logic Framework – Custom Logic Support

Quadia provides two large FPGAs for custom code implementation. Innovative Integration provides source code of the logic blocks implemented on the card as delivered and demonstrating hardware functionality:

- DSP interfacing through EMIF-B buses and McBSP ports
- Digital IO connections to PMC site P4 connector
- SBRAM and SDRAM controllers
- Load mechanism routed through the central-FPGA
- Inter-processor cross point switch communication
- Serial FPDP port with bidirectional data flow

These blocks consumes less than 15% of the VP40 device and constitute the logic frame work from which custom logic development will stem. VHDL source files as well as test bench files for ModelSim are provided to customers. Control files are also provided for pin use and timing constraints. Development is supported using Xilinx ISE, XST VHDL, with simulation under Mentor Graphics ModelSim.

The Velocia -FPGA is not intended for end-user logic development and source code is usually not provided to end-users. Contact Innovative Integration if your application might require changes to these specific interfaces.

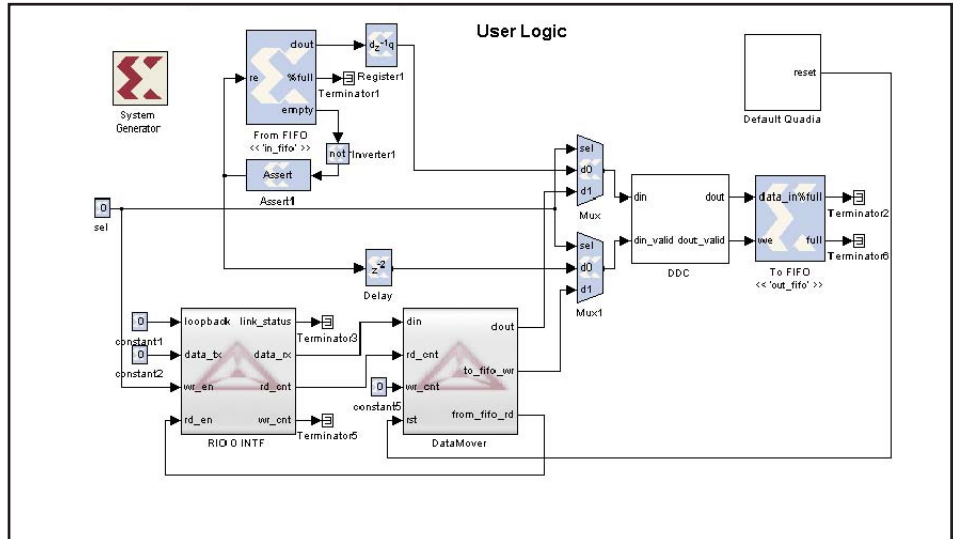
Software and Logic Framework – Custom Logic Support

Quadia offers a 4M gate FPGA for custom code implementation. Innovative Integration provides source code of the logic blocks implemented on the card as delivered and demonstrating hardware functionality: DDR SDRAM control, SBSRAM controller, Pn4 interface, XMC interface and interface to the PCI-FPGA.

Logic development is supported using either VHDL and/or MATLAB. VHDL source files as well as test bench files for ModelSim are provided to customers. Control files are also provided for pin use and timing constraints. Development is supported using Xilinx ISE, XST VHDL, with simulation under Mentor Graphics ModelSim.

MATLAB Simulink, in conjunction with Xilinx System Generator may be used for logic development. This powerful tool set allows the signal processing designer to develop algorithms using all the power and grace of MATLAB and then implement them directly in logic. The Framework Logic provides blocks for the hardware interface ready to use in the Simulink graphical design environment. Gateways to MATLAB allow the developer to quickly test the system by using Simulink to generate, analyze and display the actual data on the hardware during design. Nothing could be easier for advanced signal processing development!

The PCI-FPGA is not intended for end-user logic development and source code is usually not provided. Contact Innovative Integration if your application might require changes to these specific interfaces.



A typical block diagram design using MATLAB

MATLAB Examples

MATLAB Example	Demonstrates
SBSRAM Use	Configuration of reading and writing data through the interface.
DDR	Use of DDR as a FIFO and data flow controller using Data Mover.
Rocket IO	Configuration to loopback data through four Rocket IO interfaces.
PMC_J4	Configuration to loopback data through PMC_J4 interface.
DSP_Interface	Use of DSP0 to send data, loopback the data through RIO 0, and capture data before entering DSP0 read FIFO.
Digital Down Converter	Design flow about how to implement a DDC, hardware cosimulate in Quadia, and integrate the design into FPGA.



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Digital Signal Processor

Four TMS320C6416 at 1GHz
 32-bit fixed-point DSP
 16KB L1 Data Cache
 16KB L1 Data Cache
 1MB L2 unified RAM/Cache
 (3) 32bit timers
 64 EDMA channels

Memory

32MB SDRAM private, on each processor
 Mapped on 64-bit EMIFA, 133MHz bus clock
 Optional 2MB SBSRAM on each user-FPGA
 Optional 32MB DDR SDRAM on each user-FPGA
 64MB Global DDR SDRAM on PCI bus

PMC/XMC site

Two sites 64bit/33MHz
 Jn4 connected to FPGA digital IO (64 pins + 8 other pins, default LVDS)
 Local PCI bus to PMC 64-bit/33MHz/3.3V
 4 lanes of Rocket I/O @ 2 Gbps
 Two units, each connected to both FPGAs
 800 MB/s between XMC Site and FPGA
 Complies with VITA 42.0

FPGA

Two Xilinx XC2VP40 VirtexII-Pro
 Xilinx XC2VP40-5FF1152C standard
 85% available for end-user code
 Connects to DSP via EMIF-B and two McBSP
 Connects 64 pins to Jn4 of PMC site + 8 other pins
 4 Rocket I/O connections to XMC site
 Dual Rocket IO lanes to Velocia FPGA
 FPGA to FPGA communication up to 800MB/s
 External clock SMB input
 One LED each
 4-bit direct link between user-FPGAs for sync signals
 44 FPGA direct connections to cPCI J5 for expansion/debug
 Xilinx XC2VP50 optional

PCI Interface

64bit/133MHz PCI-X
 PICMG 2.1 compliant
 Compatible with 64/66, 64/33, 32/33
 3V/5V compatible
 Bus master or target operation
 Busmaster burst rate to 528MB/s

External Data Ports

J5 connector has 44 direct connections to each VP40 FPGA
 May be used for application-specific rear-terminal cards
Jn4 connectors (64pins) on each PMC site
 see PMC Section

Ethernet Ports

Two ports on PMC per PICMG 2.15
 Routed to backplane per PICMG 2.16 (no PHY)

Data Plane Communication

Implemented in VirtexII-Pro
 Connects EMIF-B of DSP, VirtexII-Pro, external serial ports, PMC Sites
 266 MB/s at DSP burst interface
 2 Gbps (higher speed grade logic devices support up to 3.125 Gbps)
 400 MB/s between PMC Site and FPGA over J4
 Two SFP Ports at 2.5Gbps each
 800 MB/s using XMC to FPGA

PLL Timebase

25-800MHz
 3pS rms jitter
 14.4MHz TCXO 5ppm crystal

PICMG 2.16 PSB Support

PMC/XMC site 1 supports dual Ethernet connections to the backplane
 Supports communications PPMCs

Physical Size

cPCI • 6U single slot

Power Requirements

14.5W typical for Framework Logic
 +5V@ 2.1A , +3.3V@ 1.4A

Cooling

Forced air required (5 CFM min)

Development Languages

DSP

C/C++ or assembler using CCStudio and Pismo toolkit

Host

MS VisualC++ or Borland C++ Builder

FPGA

Xilinx ISE tools, ModelSim test bench, VHDL FrameWork Logic, MATLAB
 Xilinx System Generator

DSP Operating System

DSP/BIOS II

Support PC.O.S.

Win2000 / WinXP
 Linux

Host PC

Intel processor recommended for max speed in host applications using Armada's "Channelize Mode" and Analysis Components, which utilize MMX technology

Certifications

CE marked
 EMI and EMC
 European Standards:
 EN 55022 Class A
 EN 61000-3-3
 EN 61000-3-2
 EN 55024
 Test Report Available

Software Selection Guide for Quadia

Software Package	Description	Usage/Requirements	Recommendations
Pismo Toolset	Peripheral libraries needed for developing code on this card. Includes host applications, target examples in source form demonstrating use of peripherals on the card, DSP-BIOS peripheral device driver.	Requires CCStudio*. Windows2000/XP compatible.	Required for all first time users. Includes 1 year of technical support.
Caliente DLL	Dynamic link library (DLL) for the Quadia.	Requires ANSI-compliant C/C++ compiler. For example, Microsoft Visual C/C++ or Borland C++ Builder.	Required for interfacing Host side code to DSP. May be used without Malibu although not recommended
CCStudio 'C6000	Integrated development environment (IDE) for Target side development/debugging from Texas Instruments.	Requires XDS-510 compatible JTAG emulator for debugging capabilities.	Required for all first time users. Recommend use with Innovative Integration plug-n-play PCI JTAG emulator.
Malibu	Host side development package containing a suite of high-performance board-support libraries and support applets. Allows user to build/debug sophisticated data acq apps fully atop the MS Windows graphical environment quickly with Innovative Integration's Visual Component Libraries (VCL) or MFC Classes.	Requires Borland C++ Builder 6.0* or Microsoft Visual C++ 7.0.	Recommended for inexperienced and seasoned C/C++ programmers. Offers easiest interface while providing the most flexibility and performance. Ties into a plethora of 3rd party libraries.

The Quadia Development Package contains all software packages listed above.

*Contact Innovative Integration for current release version.