

RF - Ultra High Speed Analog I/O Module

The two input channels employ Analog Devices AD9226 A/D converters with 12-bit resolution at up to 65 MHz. The input signal processing chain consists of 50 Ohm input termination, a high speed low distortion input amp, an optional programmable gain amp giving a signal amplification range of -14 dB to +34 dB, followed by a 7th order low-pass filter to the A/D. The two's complement data from the A/D converters clock into 1 KWord FIFOs, which are configured to interrupt the host card at programmable levels. Clocking is provided to the two A/Ds using either the onboard dual channel DDS, the host DDS or an external clock source (TTL or LVDS).

The two analog outputs commission Analog Devices AD9765 12-bit, D/A converters. Each channel includes a 7th order low-pass filter, an output buffer amp and has a single-ended output matched to 50 Ohms. The DACs are directly fed by a 1 KWord FIFO and triggered by the onboard DDS or an external clock source. The DAC FIFO levels are monitored in a FIFO status register and can trigger interrupts to the host card.

Digital gain and offset correction are done in real-time in the FPGA for both the A/D and D/A channels. The RF module also has the ability to stack the data samples in order to maximize the use of its 32-bit word length and increase the overall sample rate. This means two samples of a 12-bit channel can be stacked on the 32-bit word to double the OMNIBUS bandwidth or 4 samples of 8 most significant bits can be stacked to quadruple the read/write rate. (See baseboard data sheets for bandwidth specs.)

Four pairs LVDS of digital I/O are pinned out directly from the FPGA to the OMNIBUS connector for general digital handshake or high-speed interfaces.

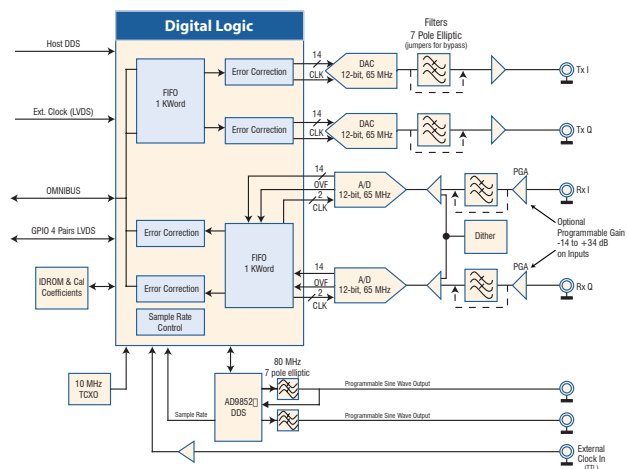
Software examples demonstrating module operation and communication are included in the Zuma/Armada Toolsets. A full calibration report ships with every module.

Ordering Information

RF (without programmable gain)	80020-24
RF (with programmable gain)	80020-24A
SMB to BNC Cable	67021

Bus type	Compatible with all OMNIBUS host products Consumes one interrupt to host
Power Requirements	2W
Physicals	OMNIBUS mezzanine card; 2.0" x 4.6"
A/D Converters	2 Analog Devices AD9226 converters
Resolution	12-bit
Update Rate	65 MHz max.
Analog Input Range	±1V at 0dB; +40dB with programmable gain amplifier
Analog Input type	Single ended to 50 Ohm SMB connector
Analog Input Impedance	50 Ohm
Input Filter Characteristics	Lowpass or Bandpass 7 pole; -3 dB point @12 MHz May be bypassed
SNR	>64 dB (without variable gain); >53 dB (with variable gain)
SINAD	45 dB (with variable gain)
THD	<0.01%
Conversion Trigger Sources	On board or host board DDS or external clock (TTL or LVDS) Optional dither on A/D for improved S/N
Interface to Host Card	Memory mapped configurable 32-bit result
D/A converter	Analog Devices AD9765 converters
Resolution	12-bit
Output Range	±1V
Settling Time	35 ns
Dynamic Range	72dB
THD	0.01%
Offset Error	Software controlled digital trimming on each channel - factory calibrated
Gain Error	Software controlled digital trimming on each channel - factory calibrated
Interface to DSP	Memory mapped 32 bit result, programmable via logic
DDS - AD9852	200 MHz input with 40 bit resolution in frequency max. Maximum DDS output rate is 80 MHz
TCXO	5 ppm TCXO (10 MHz) onboard

Digital I/O 4 pairs LVDS (2 in, 2 out) on OMNIBUS Connector



In System Performance

