



SBC6713e

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10/100 Ethernet Connectivity
300MHz TMS320C6713 DSP
600Kgate Spartan-IIe FPGA
Dual OMNIBUS I/O Sites

Overview

SBC6713e is a high-performance, flexible, stand-alone DSP board with Ethernet connectivity, loaded with I/O peripherals. Built around the powerful, C-friendly, 300MHz floating point C6713 DSP, it is a fully open platform with 15+ OMNIBUS available off-the-shelf daughter cards that provide a wide choice of A/D and D/A and also supporting simple EMIF bus interface to custom IO daughter cards. TCP/IP is running on a dedicated DM642 co-processor to preserve the C6713 for user-code and other peripheral controls. System-level integration is facilitated with on-board digital IO, DDS timebase, external clock input, multi-card sync, FPDP Data Port data links, 2MB flash ROM and watchdog. One Spartan-IIe FPGA of up to 600 Kgates is available for implementing custom logic interfaces or hardware accelerated signal processing. In a compact 160mmx100mm 3U form factor, SBC6713e is the prime choice for high-end embedded control, remote data acquisition, industrial real-time sub-systems and sophisticated OEM instrumentation.

The card can operate 100% stand-alone, with self-booting and subsequent user-application loaded from flash ROM, and may be freely embedded in custom target systems to perform autonomous data acquisition or control functions. With a 10/100 Ethernet port and simple RS232 link, the card can also communicate with a host PC that can become a remote command and control center as well as graphical user interface and file I/O end-point.

DSP Processor Core

The SBC6713e employs a TMS320C6713 32-bit DSP, Texas Instrument's fastest floating-point DSP that utilizes all strength and maturity of the C6000 series architecture. This DSP is the engine for data movement and data processing on the SBC6713e. With 8 parallel execution units, 256KB of on-chip memory coupled with an efficient two-level cache controller and 16 DMA channels, the C6713 is recognized by developers as the most "C-friendly" processor. The software libraries provided with the card make good use of DSP/BIOS peripheral drivers to facilitate end-user code development for the most complex multi-thread applications while optimizing bandwidth utilization. The toolset includes turn-key data acquisition and playback application with source code that illustrates the best utilization of all hardware resources.

The two-level cache controller uses an L1 cache of 4KB data and 4kB instructions, and 256KB that can be partitioned via software between L2 cache and unified mapped RAM. Additional memory is provided on the board with 32 MBytes of 1 wait-state synchronous SDRAM. The enhanced DMA controller handles 16 independent channels, which greatly relieves the CPU from bulk data movement and preserve its bandwidth for application-specific code. The EMIF is interfaced via one Xilinx Spartan-IIe FPGA device that controls all peripherals. Both McBSP sync serial ports are pinned out and interfaced to the logic. A Texas Instrument TMS320DM642 fixed-point co-processor is fully dedicated to the IP stack and control of the physical interface to the 10/100 Ethernet port.

Interrupt control is in the FPGA and allows control of edge/level and source selection via software and DMA transfer count supports interrupts for block movements.

Features

- 300MHz TMS320C6713DSP (Floating Point)
- Two OMNIBUS I/O Expansion Sites
- 10/100 Ethernet, RS232 Port
- Capable of 100% Stand-Alone Operation
- 600K gate Spartan-IIe for user-code (optional)
- Wide Selection of Analog Input/Output
- FPDP Data Port 200MB/s
- 3U Size 100mm x 160mm

Applications

- Embedded Control
- Remote data acquisition
- Industrial Test & Measurement
- OEM instrumentation

Hardware Options

- Ethernet Cable
- RS232 Cable
- 100 Pin MDR Cable & Breakout
- Low Noise Power Supply



OMNIBUS Compatible

For details visit:
innovative-dsp.com/omnibus

Software Development Tools

- Pismo Toolset
- TI Code Composer Studio
- CodeHammer / Debugger



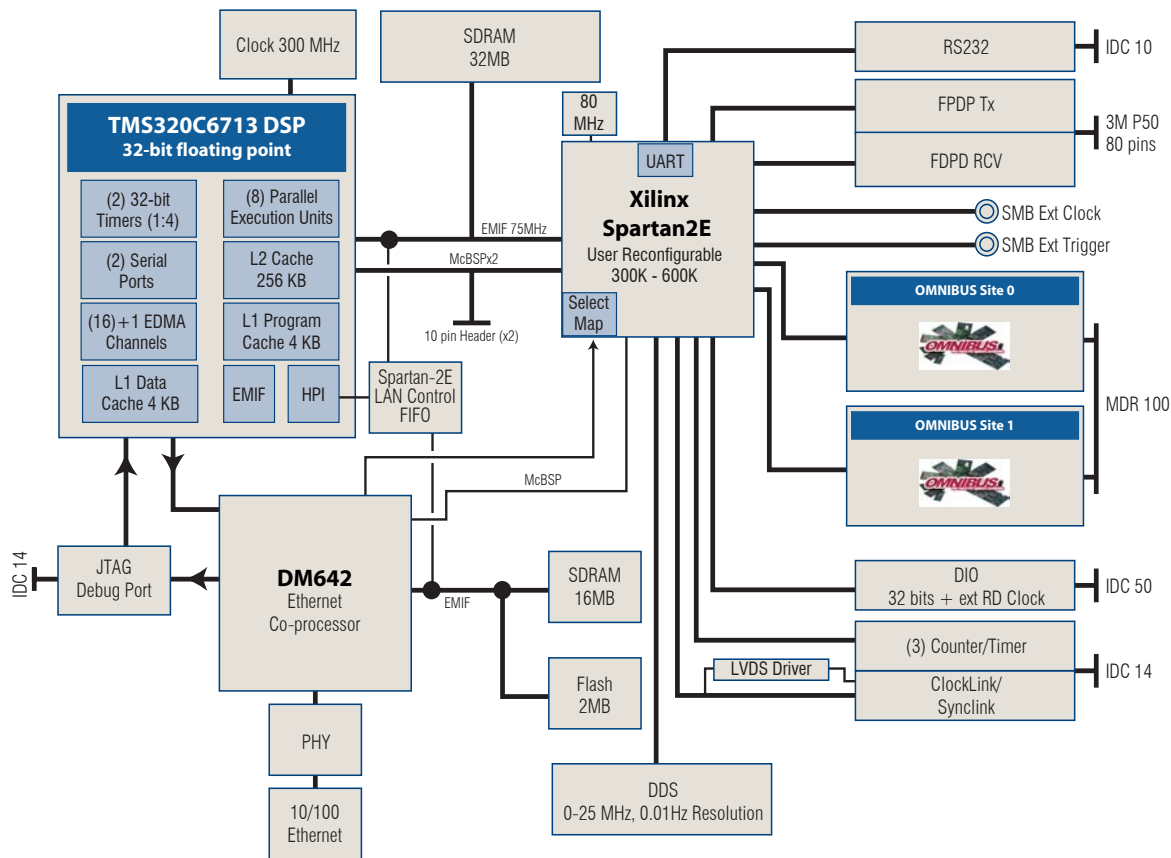
Ordering Information

SBC6713e Basic	80107-1
SBC6713e with XC2S600	80107-2



DevPack Available

For details visit:
www.innovative-dsp.com/devpack



OMNIBUS I/O Expansion Sites

System design flexibility with the SBC6713e is provided via two OMNIBUS daughter card sites that are interfaced - through the logic - to the C6713 32-bit EMIF bus. Innovative Integration offers a large family of OMNIBUS modules (daughter cards) that simply plug onto the SBC6713e board to add the desired set of analog input or output channels or high-speed digital serial interface. From simultaneous 200 kHz 16-bit A/D and D/A channels, to 65MSPS sampling for IF receive/transmit, to 100+ dB signal purity using 24-bit sigma-delta converters, the OMNIBUS family serves a very broad range of application, off-the shelf. System integrators may also design custom daughter card for installation on the SBC6713e to address very specific application requirements. OMNIBUS is an open bus architecture that is flexible, easy to use and high-performance. It is a 37.5MHz synchronous parallel bus structure utilizing four decode (chip select) signals per site with 12-bit sub-addressing available. Module may be memory mapped into the DSP memory and drive multiple independent interrupt signals back to the DSP. Numerous timing, power and handshaking signals are provided. Full description of the specification is available on our web site.

ON-BOARD PERIPHERALS AND SYSTEM-LEVEL FEATURES

Digital I/O

A simple high-speed memory-mapped, 32-bit latch is available to support general-purpose LVTTTL digital I/O, with ESD and overvoltage protection. Direction is software-configurable in bytes. The port may be software or externally clocked at rates to 20 MHz.

Accurate DDS Timebase

The output of an AD9851 digital synthesizer is routed to the logic, where postscaling reduces jitter before presenting a very stable time base to both OMNIBUS sites. It provides a 0-25MHz time base programmable in .01 Hz increments.

RS232

A 1200 to 38.4kbaud asynchronous serial port is provided for simple connectivity, interface to dumb terminal or other hardware. The UART is implemented in logic.

FPDP Tx/Rcv Data Port

This private data path offers high-speed dedicated parallel board-to-board communications between the SBC6713e and other FPDP compatible cards and hardware at rates to 200Mbytes/sec. The FPDP conforms to VITA 17 and is a simple protocol consisting of 32-bit data plus flow control signals and clock up to 50 MHz. FIFO buffering is provided on the SBC6713e Receive Port.

External Clock and External Interrupt Inputs are available on SMB co-ax connectors.

Multi-card synchronization

The SyncLink/CiKLink interface allows up to four unique timing signals and event triggers to be shared between up to 16 cards. The SBC6713e has a switch matrix that routes any event trigger to any SyncLink/CiKLink port, completely under software control. For instance, the DDS output can drive an LVDS pair to serve as external clock to other cards. There is no complex cabling, just a simple connection and software configuration.

Network Connectivity and Booting

The SBC6713e features a dedicated DSP co-processor - TMS320DM642 - that is fully responsible for Ethernet port protocol and data flow and ensures an "always on" communication that is easy to configure and use. The co-processor resource include 16MB of SDRAM, 2MB flash, and performs TCP/IP and data buffering. The port is capable of a continuous 100Mbps data flow - though this includes TCP overhead.

EMIF interfaces are used to move data between the C6713 and DM642, using DMA channels and FIFO buffering in logic. This efficient method reduces burden on the 6713. The software framework provides user-friendly communication commands to control block movement of data that is used for continuous data streaming as well as command and control.

The DM642 also ensures a reliable booting process of the SBC6713e. The DM642 boots first from flash, loads the Spartan-IIIE logic and finally is able to load the 6713, over HPI, with an application program. Subsequent to booting, the DM642 acts as the Ethernet host to the 6713 by managing Ethernet traffic, being able to reset the 6713 and load new applications or new logic images.

User-Reconfigurable Logic

The SBC6713e is offered with optional user-reconfigurable logic, with pin-compatible Spartan-IIIE device of up to 600K gates. The existing logic image of the basic functions and interfaces described herein consumes around 17% of the device, leaving ample resources to implement custom digital interfaces, ultra-fast data formatting/merging or even hardware-accelerated signal processing. The VHDL source code of the "stock" logic is provided as a basis for further development of customer-specific customization to suit the end application or serve as an aid in the understanding of the external interfaces and some high-efficiency data flow schemes. FPGA code development expertise and the Xilinx development tools are required for such development.

Software Tool Suite

The SBC6713e Pismo tool kit is a powerful collection of software libraries, utilities, examples projects and interactive help file that allow developers to be very productive from the start. Numerous program examples - with source code- demonstrate the usage of every peripheral on the board as well as OMNIBUS expansion modules. Pismo provides a framework for flexible and high-bandwidth communication with a PC over 10/100 Ethernet link, and offers handy utilities that simplify board utilization and truly accelerate system development.

Target Side Tools

Extensive C/C++ libraries, example source code, DSP/BIOS peripheral drivers, mailbox messaging and bulk data transfer to/from PC are fully integrated in Texas Instrument Code Composer Studio. Pismo makes extensive use of DSP/BIOS, TI's DSP operating system included in CCStudio, which simplifies code development of complex, multi-thread applications by providing drivers, scheduling services and run-time management of all DSP resources to optimize bandwidth. Users do not need to understand hardware-specific low-level code to set up and control IO peripherals. Another benefit of DSP/BIOS is a modular, easy to maintain code structure, well ahead of an old fashion, complex, main() program to structure task priorities and dependencies. At debug time, DSP/BIOS also provides real-time profiling to aid in optimizing code.

The MathWorks MATLAB and Simulink packages allow developers to work in an interactive graphical environment and use a customizable set of block libraries to design, simulate, and test sophisticated algorithms, The MathWorks Real time Workshop Embedded Coder for C6000 DSP can then generate C-code for a specific DSP Chip. The output files are then easily cross-compiled with board-specific libraries under Code Composer Studio and are ready to run on the Innovative Integration hardware.

Host Side Tools

Pismo includes two groups of Host Side support tools: extensive C++ libraries -with sophisticated program examples- and turnkey utilities. Libraries include methods to control the SBC6713e (Reset DSP, Download code) and to communicate with the board via mailbox-style messages or bulk data transfer. Both communication techniques are very intuitive and well illustrated in examples. Turnkey utilities - provided as executables - facilitate board utilization and program debugging at the beginning of a project. UniTerminal is a dumb terminal emulator ~similar to Windows console mode ~ giving an out-of-the-box user interface to the DSP programmer for text display, keyboard entries and even file I/O, and handles board reset and code download. DSP developers can immediately write DSP code and defer the host-side work. BinView is a binary data viewer that graphs and analyzes data in time and frequency domains, and can be directly invoked from within UniTerminal. All of these tools can co-exist, at run-time, with Code Composer Studio Debugger. In fact, many users prefer to use Pismo utilities over Code Composer Studio's RTDX data exchange scheme because of higher bandwidth and user-friendliness.

OEM Configurations

The SBC6713e can be configured or modified to fit your specific requirements and provide an optimal mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.

SBC6713e Technical Specifications

Digital Signal Processor

300MHz Texas Instruments TMS320C6713 floating-point DSP

On-chip resources

L1 cache 4KB data/4KB program
L2 cache + Unified RAM 256 KB
Two multichannel buffered serial ports
Two 32-bit timers
Sixteen DMA channels
32-bit external memory interface

FPGA

Spartan-IIe 300K-gate (XC2S300E) not reconfigurable by end-user
Spartan-IIe 600K-gate (XC2S600E) fully reconfigurable by end-user with Xilinx ISE tools and SBC6713e logic framework (framework provided free of charge)

Memory

32 MBytes synchronous DRAM (1 wait-state)
2MByte Flash ROM

Debug Port

JTAG 1149.1 compliant emulation port
Compatible with Innovative Code Hammer, TI XDS-510, or equivalent debugger using TI Code Composer Studio.

Ethernet Port

10/100Mbps capability
Full TCP/IP support

Digital I/O

32-bit programmable as input or output by byte
LVTTTL, direct from FPGA

FPDP Tx/Rcv Ports

200MBytes/sec bidirectional data path
FIFO memory: 256x32
32-bit data points
Up to 50 MHz clock
Conforms to ANSI/VITA 17

RS232 UART

Asynchronous Serial Port, full duplex
Interrupt driven communications
RS232 driver compatible with PC serial port
Rates: 1200, 2400, 4800, 9600, 19200, 38400
Data Format: 8-bit
Transceiver: Maxim Max3223

Timers/Counters

Two on-chip, 32-bit timers

Clock Generation

One programmable digital frequency synthesizer AD9851
0-25 MHz range in 0.01 Hz steps.

Multi Card Synchronization

Synchronize multiple SyncLink cards to a common trigger or clock
Software selection for master/slave card function
Two High speed LVDS signals for clocks
6 TTL compatible signals for triggers.

OMNIBUS I/O Module Sites

Two OMNIBUS module sites
Expansion using OMNIBUS modules for analog and digital I/O Compatible with all OMNIBUS modules.
50 module-specific I/O connections per module.

OMNIBUS Bandwidth

Up to 16 MHz accesses on 32-bit bus

Connectors

IDC-40 polarized male pin header for digital I/O
IDC-14 polarized male pin header for JTAG emulation
Two 3M P50E 80 pins for FPDP Tx/Rcv
RJ-45 for 10/100 Ethernet
IDC-10 for RS232
6-pin latching power connector -Molex 43045-0602
One 100-pin MDR connector for I/O modules
IDC-10 polarized male pin header for SyncLink/ClockLink
2 BNC connectors for external clock & interrupt

Physical Description

3U card - 100 mm x 160 mm
Max card height with modules - 1.5 in
Power Requirements
+5 V @ 1.1 A,
Does not include +5V and ±15 V for modules

Operating Conditions

10-55 degrees C
Some configurations may require forced air

Development Languages

DSP

C++ or Assembler for DSP under Code Composer Studio
Pismo Toolset includes libraries, projects, utilities, help files
MATLAB/Simulink for graphical algorithm development and DSP code generation

PC

Borland C++ Builder, MS Visual C++, .NET
DSP Source Code Debugger and Real Time Profiling
XDS510 compliant JTAG with Code Composer Studio Debugger

DSP Operating System

DSP/BIOS II



Kane Computing Ltd
7 Theatre Court, London Road,
Northwich, Cheshire, CW9 5HB, UK.
Tel: +44(0)1606 351006
Fax: +44(0)1606 351007/8
Email: sales@kanecomputing.com
Web: www.kanecomputing.co.uk