

GSM wireless BTS reference design

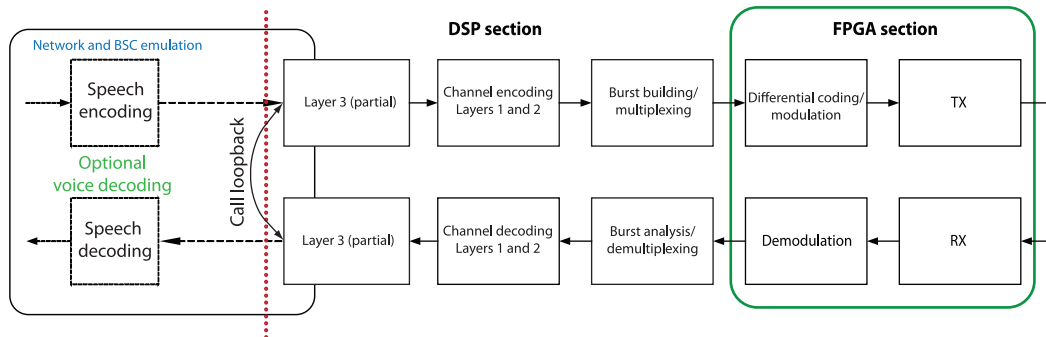
Reference sheet

This Lyrtech reference design is a DSP–FPGA-based GSM design showcasing the powerful combination of a high-end DSP (the Texas Instruments DM6446 digital media SoC) and Virtex-4 FPGA. The implementation shows how these advanced processing devices can be applied to software-defined radio processing in an embedded wireless device. The reference design runs on the Lyrtech Small Form Factor (SFF) Software-defined Radio (SDR) development platform, developed with Texas Instruments and Xilinx.

The GSM wireless BTS reference design is a simplified GSM base transceiver station. It uses the Lyrtech GSM protocol stack and establishes basic communications between two GSM devices and the SFF SDR development platform that emulates a base transceiver station (BTS) and network functions (below). It provides most of layer-1 and layer-2 modules for the DSP and FPGA, while layer-3 modules are implemented for basic BTS demonstration purposes. The design uses a mixed design flow—where the protocol layer targeted at the DM6446 is implemented in C/assembly and the physical layer targeted at the FPGA (all this

AT A GLANCE

- Sets up a call and loopback between two mobile GSM phones
- Applies ETSI GSM recommendations
- Targets the Lyrtech SFF SDR development platform
- Best for pico BTSs, GSM monitoring systems, GSM-based sensors, and advanced reprogrammable multimode/SDR handheld communication devices



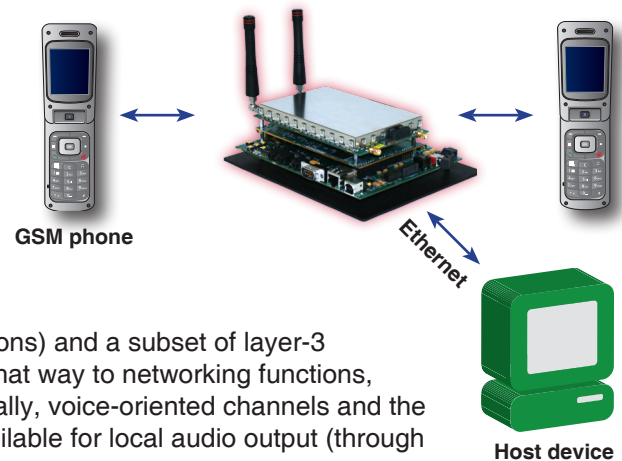
DSP–FPGA GSM partitioning, BTS emulation mode

The DSP performs the necessary baseband processing (above) with the Lyrtech GSM protocol stack and DSP libraries. Layer-2 and layer-3 event-driven code also runs on the DSP, but could as easily run on the adjacent ARM processor. A host application allows monitoring the BTS emulation activity through an Ethernet link.

Typical setup

Two GSM mobile phones communicate with each other through the SFF SDR development platform, emulating a GSM BTS. A monitoring and configuration program runs on a host device connected to the SFF SDR development platform through an Ethernet link, as illustrated here.

The illustration above shows the main components of the system and the DSP–FPGA processing partition.



Baseband and protocol processing

Most layer-1 and layer-2 messages (mainly the ones for voice communications) and a subset of layer-3 messages are implemented (next page). Implementing layer 3 also opens that way to networking functions, making a complete call setup between two mobile devices possible. Optionally, voice-oriented channels and the voice coders/decoders necessary to GSM voice decoding can be made available for local audio output (through AMR coders implemented with Lyrtech DSP-optimized C-code libraries).

is accomplished using a model-based design flow).

The target platform is the modular SFF SDR development platform, which is equipped with a baseband DSP–FPGA module, a high-speed sampling module (used to sample the intermediate frequencies (IF)), and an RF front end. The FPGA performs the necessary IF processing, which is implemented with Simulink and System Generator for DSP.

Layer-3 messages include the following messages (ETSI-recommended primitives are also used):

Subset

- CALL CONFIRMED, CALL PROCEEDING
- CONNECT, CONNECT ACKNOWLEDGE, DISCONNECT
- SETUP
- ALERTING
- RELEASE, RELEASE COMPLETE
- CHANNEL REQUEST, RELEASE
- PAGING REQUEST, RESPONSE
- ASSIGNMENT COMMAND, COMPLETE, IMMEDIATE ASSIGNMENT
- CHANNEL MODE MODIFY, CHANNEL MODE MODIFY ACKNOWLEDGE
- ACKNOWLEDGE

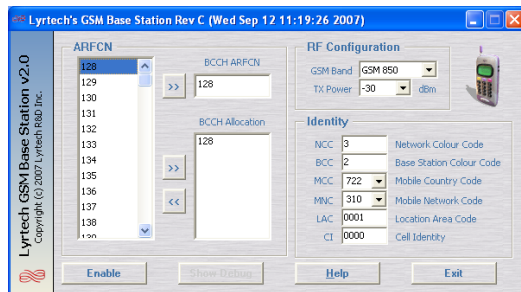
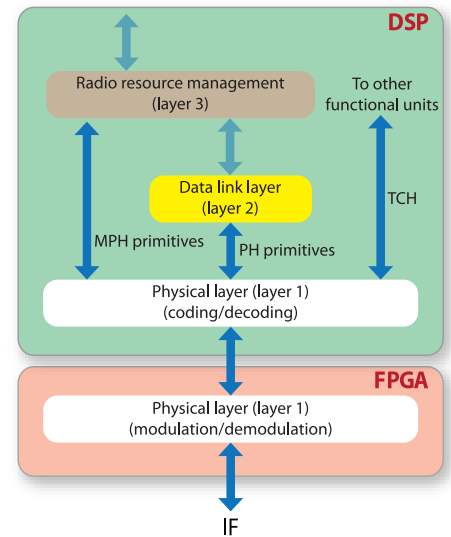
Primitives

All inter-layer primitives are implemented:

Layer 1–3 primitive: MPH INFO

Layer 1–2 primitives: PH DATA, PH RA, PHRA CONFIRM

Layer 2–3 primitives: DL DATA, DL UNIT DATA, DL ESTABLISH, DL RELEASE, DL RANDOM ACCESS INDICATION



Monitoring software

The reference design also comes with a host software program used in setting up the BTS and monitoring its activity through a simple interface (left).

From the interface, users can select frequency channels, as well as select a mobile country code (MCC) and mobile network code (MNC). In the example at the right, the MCC is set to 722 (Argentina) and the MNC to 310 (CTI).

Proportion of resources used by the reference design

The reference design uses approximately 60% of the logic slices, 30% of the BRAM, and 20% of the DSP48 slices of the Virtex-4 SX35 FPGA of the SFF SDR development platform. It also uses approximately 20% of the available DSP MIPS.

FOR MORE INFORMATION



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