

ADACMaster III

Add-on module for the SignalMaster Dual and SignalMaster Quad

The ADACMaster III is a LYRIO add-on module designed for Lyrtech's SignalMaster Dual and SignalMaster Quad. The ADACMaster III is a phase-synchronous, dual-channel, ADC/

AT A GLANCE

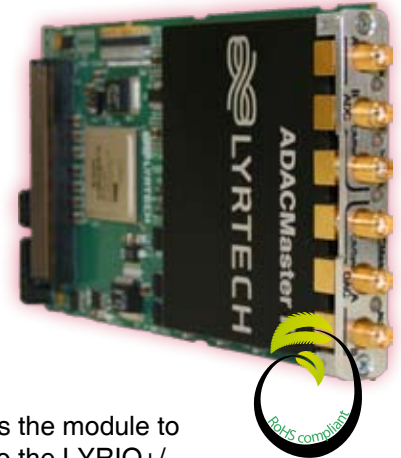
- Very-high-speed LYRIO module
- Two 125-MSPS, 14-bit, analog-to-digital converters
- Dual-channel, 500-MSPS, 16-bit, interpolating digital-to-analog converter
- Onboard preprocessing and post-processing LX/SX Virtex-4 FPGA
- Multiple high-performance clock sources and synchronization options
- Support for model-based design flow

DAC module designed to bring new levels of performance and flexibility to a wide variety of signal processing applications, including advanced telecommunications, software-defined radio, testing and measurement, medical applications, and more. Such data-intensive applications benefit from the module's two 14-bit ADCs capable of sampling at up to 125 MSPS; the dual-channel 16-bit, 500-MSPS interpolating DAC; and the optimized system synchronization.

The ADACMaster III is also equipped with one onboard Virtex-4 FPGA (LX25 or SX35) that allows the module to preprocess incoming data before it is transferred to the LYRIO+/LYRIO carrier board (post-processing from the carrier board is also possible). The Virtex-4 FPGA is capable of delivering up to 96 GMACS of FPGA-based DSP processing power—unrivalled might at your fingertips.

Combining the ADACMaster III with the DSP-FPGA processing engines of the SignalMaster Dual and SignalMaster Quad yields a complete and very-high-performance IF/baseband solution.

The ADACMaster III comes with a complete board software development kit that makes its easy to design and test complex algorithms. It is also possible to simultaneously design and test in a real-time environment through the module's integration to the model-based design software tools for Simulink.



Optimized system synchronization

- Clock synchronization circuit for the ADC/DAC, with clock phased-locked to an internal or external reference clock
- AD9511 clock synthesizer synchronizes the VCO frequency to the reference clock
- Two independent external clock inputs are available for optimized ADC and DAC performances
- Available external triggering and synchronization input circuitry for event-based applications

Easy analog front end integration and circuitry

- High sampling rate—125-MSPS ADCs and 500-MSPS DAC
- 35-dB software programmable linear gain/attenuation control on each input channel (when equipped with the AC-coupled option)
- 32 GPIO signals for analog front end remote control or other user-defined applications



Stellar processing power

The 34,560 logic cells and 192 XtremeDSP slices of the Virtex-4 SX35 FPGA make meeting the highest processing needs surprisingly easy.

Integrated to System Generator for DSP

The ADACMaster III is fully integrated to System Generator for DSP from Xilinx, which allows using high-level abstractions that can be compiled automatically into the FPGA without losing any performance over designs implemented with VHDL.

Better accuracy

The ADACMaster III is extensively shielded, which gives it excellent between-channel and external noise insulation (up to -100 dBc inter-channel crosstalk insulation).

Features

The ADACMaster III offers the following features:

- Two 14-bit, 125-MSPS input channels
- Two 16-bit, 500-MSPS output channels
- Multiple clock sources—two external clock inputs (ADC and DAC), onboard synthesizer (optional external reference), and tight clock synchronization circuit
- A Xilinx LX25 or SX35 Virtex-4 FPGA that offers unsurpassed capabilities and high-performance logic
- An onboard flash PROM that simplifies booting the FPGA
- An array of tools that allows designing complex algorithms for the ADACMaster III such as block models with the popular MATLAB and Simulink programs
- The ADACMaster III is also compatible with one of the most powerful integrated development environments on the market—ISE Foundation
- A GPIO-32 port with 32-bit user I/O header routed to the onboard FPGA
- Independent, software-programmable gain amplifier/attenuator on each acquisition/transmission channel (with the exception of the DC-coupled option for the input channels only, which have a fixed unity gain)

Applications

The following are a few applications where the ADACMaster III truly shines:

- Software-defined radio
- Advanced base stations
- 2x2 smart antennas, multichannel IF systems
- Cable modem termination systems
- Radar and sonar
- GPS anti-jamming receivers
- High-speed testing and measurement systems
- Channel analysis (recording and playback)
- Medical equipment

Software development tools

The ADACMaster III comes with the following development tools:

Lyrtech board support packages

The ADACMaster III module's flash PROM comes preloaded with an application that loads the FPGA of the module when it starts. This application allows the propagation of data from the A/D and D/A channels to the LYRIO interface and configuration path which, in turn, allows data to be directly exchanged with a carrier board such as the SignalMaster Dual and the SignalMaster Quad.

ADACMaster III board software development kit

The ADACMaster III board software development kit (BSDK) allows targeting the onboard FPGA through ISE Foundation projects. The kit also comes with detailed FPGA core documentation and a complete set of hardware functional examples that illustrate how to use the module's onboard I/Os and interfaces.

ADACMaster III model-based design kit (optional)

The optional ADACMaster III module's model-based design kit (MBDK) allows targeting the onboard FPGA using System Generator for DSP from Xilinx and Simulink. The MBDK also comes with a complete set of hardware functional examples that illustrate how to use the module's onboard I/Os and interfaces in a model-based design environment.

Communication and configuration from the carrier board (supplied with the carrier BSDK and MBDK)

The BSDK and MBDK of the SignalMaster Dual and SignalMaster Quad include the necessary software to transfer data between the carrier's FPGAs and the ADACMaster III. They also come with DSP APIs (for BSDK users) and blocksets (for MBDK users) to control the ADACMaster III's parameters.



ADACMaster III on a
SignalMaster Quad

Hardware options

FPGA packages

- ADACMaster III Light—features an LX25 Virtex-4 FPGA
- ADACMaster III Advanced—features an SX35 Virtex-4 FPGA

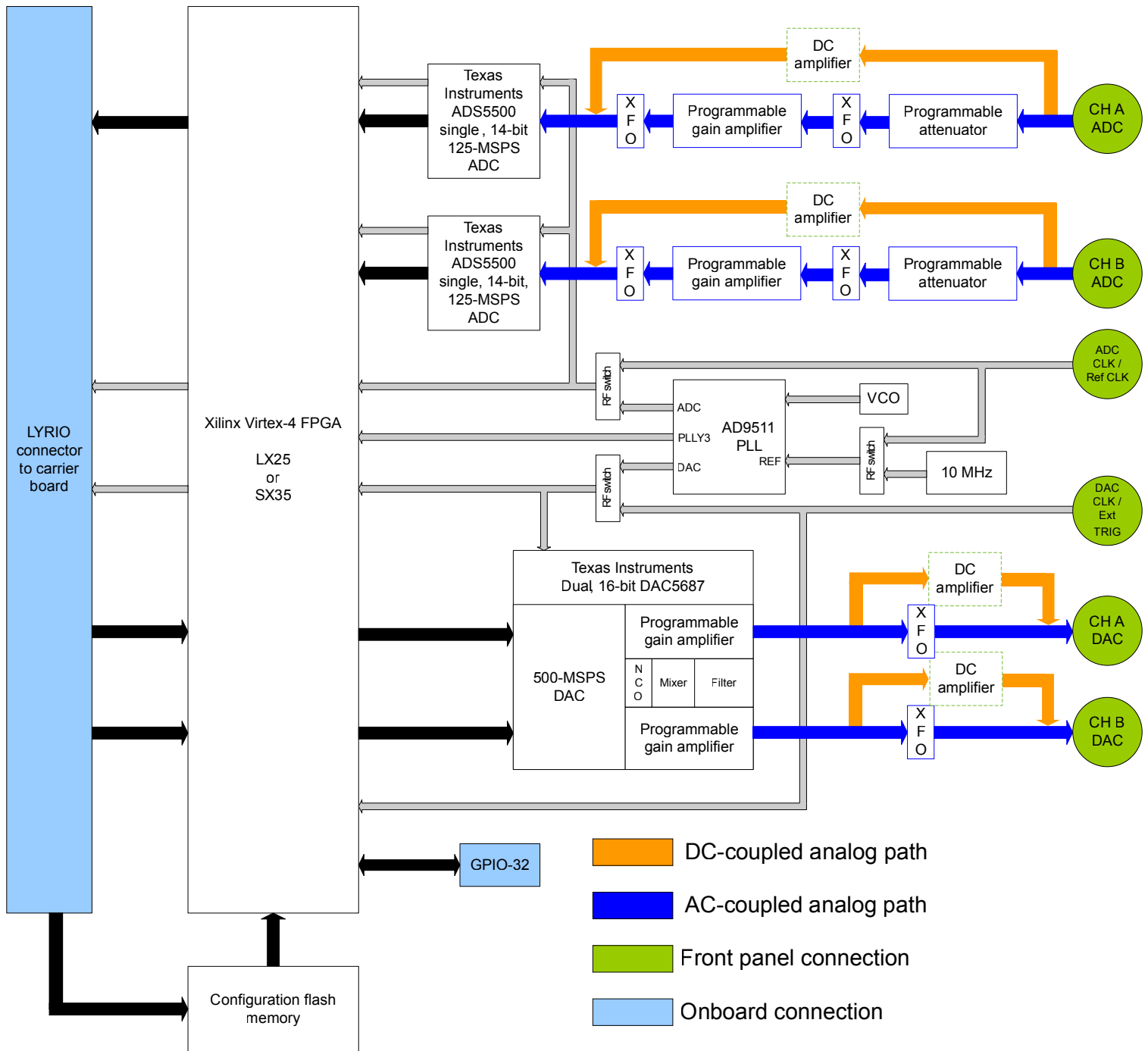
I/O packages

- AC-coupled I/O—features AC-coupled A/D and D/A channel analog paths. Under this configuration, all the input and output channels have independent programmable gain amplifiers or attenuators.
- DC-coupled I/O—features DC-coupled A/D and D/A channel analog paths. Under this configuration, all the output channels have independent programmable gain amplifiers; analog input channels **do not** have programmable gain amplifiers or attenuators. Interpolating D/A also have limited performance at high analog output frequencies.

Specifications

Analog-to-digital converters	<ul style="list-style-type: none"> • ADS5500 from Texas Instruments (x2) • Guaranteed maximum sampling rate of up to 125 MSPS (14-bit resolution)
Analog inputs	50-Ω SMA connectors
Optional analog inputs	<p>AC coupled</p> <ul style="list-style-type: none"> • 1-MHz to 150-MHz analog input bandwidth (–3 dB) • –24.2-dBm to 6.4-dBm full-scale input (depending on the programmable gain/attenuator settings) • 88-dBc SFDR at 70 MHz F_{in} (for a bandwidth of 30 MHz and a gain of 8.5 dB) • 77-dBc SFDR at 70 MHz F_{in} (for a bandwidth of 30 MHz and a gain of 31 dB) • Interchannel crosstalk insulation of 92 dBc at 70 MHz F_{in} (with a gain of 10 dB) • Interchannel crosstalk insulation of 72 dBc at 70 MHz F_{in} (with a gain of 31 dB) <p>DC coupled</p> <ul style="list-style-type: none"> • DC to 65-MHz analog input bandwidth (–3 dB) • 10.6-dBm full-scale input (no programmable gain/attenuator available) • 105-dBc SFDR at 1 MHz F_{in} (for a bandwidth of 2 MHz) • 72.04-dBc SFDR at 30 MHz F_{in} • 88-dBc SFDR at 30 MHz F_{in} (for a bandwidth of 10 MHz) • Interchannel crosstalk insulation of 98 dBc at 30 MHz F_{in}
Dual-channel digital-to-analog converters	<ul style="list-style-type: none"> • Dual-channel DAC5687 from Texas Instruments (x1) • Guaranteed maximum interpolating sampling rate of up to 500 MSPS (16-bit resolution) • 1x, 2x, 4x, or 8x interpolating factors • Integrated NCO, mixer, and digital filters • Integrated independent programmable amplifiers per channel • Integrated quadrature mode or independent dual channel
Analog outputs	50-Ω MMCX connectors
Optional analog outputs	<p>AC coupled</p> <ul style="list-style-type: none"> • 0.3 MHz to 240 MHz analog output bandwidth (–3 dB) • –21.4-dBm to 2.72-dBm full-scale output (minimum to maximum programmable gain) • 76.91 dBc SFDR at an IF of 30 MHz (for a bandwidth of 60 MHz, at full scale, interpolationX4, fine mixer, and an F_s of 500 MHz) • 77.21 dBc SFDR at an IF of 70 MHz (for a bandwidth of 40 MHz, at full scale, interpolationX4, fine mixer, and an F_s of 500 MHz) • Interchannel crosstalk insulation of –75 dBc at 30 MHz/70 MHz IF_{out} • SNR of 65 dB at 30 MHz IF_{out}, 59.2 dB at 70 MHz IF_{out} <p>DC coupled</p> <ul style="list-style-type: none"> • DC to 240 MHz analog output bandwidth (–3 dB) • –23-dBm to 0-dBm full-scale output (minimum to maximum programmable gain) • 75 dBc SFDR at an IF of 30 MHz (for a bandwidth of 60 MHz, at full scale, interpolationX4, fine mixer, and an F_s of 500 MHz) • 70 dBc SFDR at an IF of 70 MHz (for a bandwidth of 40 MHz, at full scale, interpolationX4, fine mixer, and an F_s of 500 MHz) • Interchannel crosstalk insulation of –53.2 dBc at 30 MHz/70 MHz IF_{out} • SNR of 54 dB at 30 MHz IF_{out}, 49 dB at 70 MHz IF_{out}
Sampling clocks, synchronization, and trigger options	<ul style="list-style-type: none"> • Software-selectable onboard or external reference clock • Software-selectable PLL or external ADC/DAC clock • Maximum 225 F_s rms output jitter onboard PLL • 1 GHz to 1.5 GHz onboard VCO to generate virtually any frequency • Phase noise of 110 dBc at 10 kHz for a 125-MHz generated clock output
Xilinx LX25 or SX35 Virtex-4 FPGA	<ul style="list-style-type: none"> • Maximum of 34,560 logic cells • Maximum of 192 XtremeDSP slices
Offboard communication channels	32-bit, user-defined external Virtex-4 single-ended GPIO-32 header
Mezzanine communications interface for carrier board	<ul style="list-style-type: none"> • LYRIO (x1) • Minimum 4 Gbps, full-duplex <p><i>For details about the specifications of this Lyrtech mezzanine communications interface, contact info@lyrtech.com.</i></p>

Block diagram



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With over 25 years of experience delivering advanced digital signal processing solutions to companies worldwide, Lyrtech serves customers across the Americas, Asia, and Europe. Lyrtech offers a full range of DSP-FPGA development platforms, as well as product development services. Lyrtech works in partnership with such industry leaders as Texas Instruments, The MathWorks, and Xilinx to deliver unsurpassed quality and support to its large OEM customer base, which includes many prestigious names of the consumer electronics, telecommunications, aerospace, and defense fields. In a world where digital signal processing technology is vital to network and wireless communications, audio and video processing, as well as electronic systems in all fields of technology, Lyrtech is an ideal partner.

Lyrtech products are constantly being improved; therefore, Lyrtech reserves itself the right to modify the information herein at any time and without notice.

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