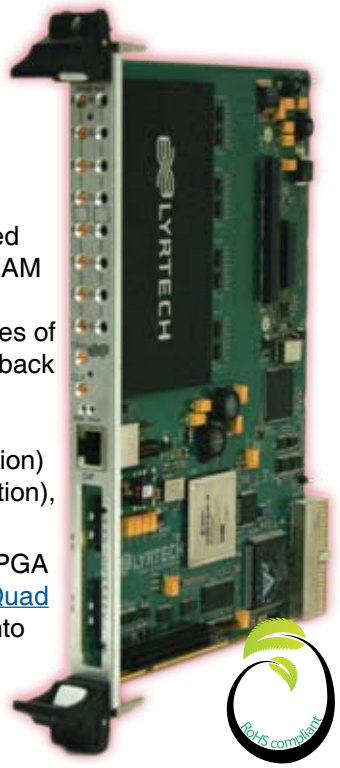
LYRTECH
Infinite possibilities...

VHS-DAC

cPCI advanced development plaform



The VHS-DAC is a high-speed, multichannel digital-to-analog conversion platform. It is equipped with eight, phase-synchronous DACs (capable of a maximum sampling rate of 480 MSPS through on-chip interpolation) and an FPGA for high-speed processing. The VHS-DAC also comes with SDRAM for data storage and an expansion connector for eight additional DAC channels or several gigabytes of DDR2 SDRAM (for simultaneous, full-speed playback on the VHS-DAC's channels). All this makes the VHS-DAC perfect for multichannel, intermediate frequency (IF) signal generation (AC-coupled option) and baseband signal generation (DC-coupled option), as well as other applications outlined herein.

Combining the VHS-DAC with additional DSP–FPGA processing platforms such as the SignalMaster Quad and SignalMaster Dual, transforms the product into a complete and very-high-performance IF and baseband solution. The VHS-DAC can also be combined with VHS-ADCs to provide an end-to-end high-speed processing chain on up to 16 channels or more.

At a glance

- Onboard, 8-channel, 480 MSPS, 14-bit DACs on 6U cPCI (PXI compatible)
- Mezzanine expansion site to support more channels or memory
- Outstanding clock synchronization
- Onboard, high-processing-speed LX/SX Virtex-4 FPGA
- Sustained 8-Gbps raw data RX/TX RapidCHANNEL ports (one each)
- Playback software tools
- Support for model-based design flow

Stellar processing power

The 256 GMACS of the FPGA allows fulfilling the highest processing needs. The family provides some of the most advanced logic, highest performance, highest density, and greatest memory capacity of other FPGA families.

Integration to System Generator for DSP

The VHS-DAC is fully integrated to System Generator for DSP, which allows using high-level abstractions that can be compiled automatically into the FPGA, without loss of performance over designs implemented with VHDL.

Multipurpose platform

Use the VHS-DAC in development cycles for:

- Data playback, which allows you to bench mark external multichannel analog equipment using signals directly created from simulation files.
- FPGA development (hardware-in-the-loop co-simulation or real-time implementation).

Reduce the risk of facing interconnection problems

Using an FPGA-based platform with eight onboard outputs helps avoid interconnection problems. The number of outputs can be expanded to 16 by adding a DAC module. The 8-Gbps, full-duplex RapidCHANNEL ports also allow adding to a system processing platforms such as the SignalMaster Quad or adding an FPDP-I/II, long-term, hard disk drive storage system capable of sustained playback at up to 200 MBps (which makes feeding large bandwidth baseband signals to the VHS-DAC possible).

Better accuracy

The VHS-DAC has outstanding clock synchronization—very-low-skew interchannel clock routing through all the DACs, optimized for tight, synchronous, multichannel signal generation applications.

The VHS-DAC is extensively shielded, which gives it excellent between-channel and external noise insulation (up to 91 dB interchannel crosstalk insulation).

Stand-alone capabilities

The VHS-DAC is equipped with an onboard flash memory for the FPGA and an I^2C/JTAG external port, making it possible to use the VHS-DAC without a cPCI CPU.

Customizable for OEM applications

Lower the cost of the VHS-DAC by requesting downsized versions of the development platform, yielding more economical production units.

Applications

The following are some of the applications where the VHS-DAC truly shines.

- Advanced base stations
- Smart antennas, multichannel IF systems, beamformers
- Wireless applications (routers, OFDM antenna diversity, Wi-Fi, WiMAX)
- MIMO space-time coding
- Software-defined radio
- High-speed, multichannel playback and signal generation
- Radar, phased-array radar, SATCOMs
- Medicine, tomography, ultrasound, and other applications

Features

The VHS-DAC offers the following features:

- Virtex-4 FPGA
  - 256 GMACS
  - 152,000 logic cells
  - 500 MHz performance
- Multichannel, 480-MSPS, interpolating DAC technology, supplied with AC-coupled or DC-coupled analog outputs (coupling option must be defined upon purchase), making it possible to reach high SNR baseband or IF signals.
- Powerful LVDS serial and parallel interface
  - **Serial digital intermediate frequency (DIF) interface**—synchronous LVDS ports (two LVDS pairs, TX/RX) on the RJ45 front panel, 105 MBps, full-duplex, based on serdes technology. The LVDS clock is linked to the acquisition frequency.
  - **RapidCHANNEL interfaces (TX ×1, RX ×1)**—LVDS ports (eight LVDS data pairs; others for synchronization and control at each port) on two Samtec Q-Pair micro coaxial connectors (TX ×1, RX ×1), 8 Gbps, full-duplex, based on the Virtex-4 on-chip serializer. The bandwidth is fixed and data is transferred through FIFO (refer to RapidCHANNEL specifications for details).
- The front panel data port (FPDP-I/II) allows data to be transferred at high speeds between FPDP-I/II-compliant hardware and can be configured as input or output through software
- Data recording and playback on the onboard 128-MB SDRAM or with a 2 GB memory module
- Stand-alone configuration through the onboard flash memory
- Language-based (C and VHDL) board software development kit
- Windows-based utility for parameter control
- Very-low-skew interchannel clock routing through all the DACs
- Unlimited multiplatform cPCI configuration. Phase synchronization is achieved by providing the same external clock to all the platforms
- Independent, software-programmable gain amplifier on each transmission channel (optional)
- Ease of development with the optional model-based design kit (optional) for MATLAB and Simulink (optional)

Software development tools

The VHS-DAC also comes with the following software development tools:

VHS-DAC board software development kit

The VHS-DAC board software development kit (BSDK) allows targeting the VHS-DAC's onboard FPGA through ISE Foundation projects and is accompanied by FPGA core documentation. Further, the BSDK includes a host API and programs that allow communicating with the VHS-DAC's FPGA. Finally, the BSDK includes a complete set of hardware functional examples that demonstrate how to use the VHS-DAC's onboard I/Os and interfaces.

VHS-DAC model-based design kit (optional)

The optional VHS-DAC model-based design kit (MBDK) allows generating code for the FPGA of the VHS-DAC from MATLAB and Simulink through System Generator for DSP. Modifying model parameters on the fly and performing FPGA hardware-in-the-loop co-simulations are also a breeze with Simulink. The MBDK also comes with a complete set of hardware functional examples that demonstrate how to use the VHS-DAC's onboard I/Os and interfaces in a model-based design environment.

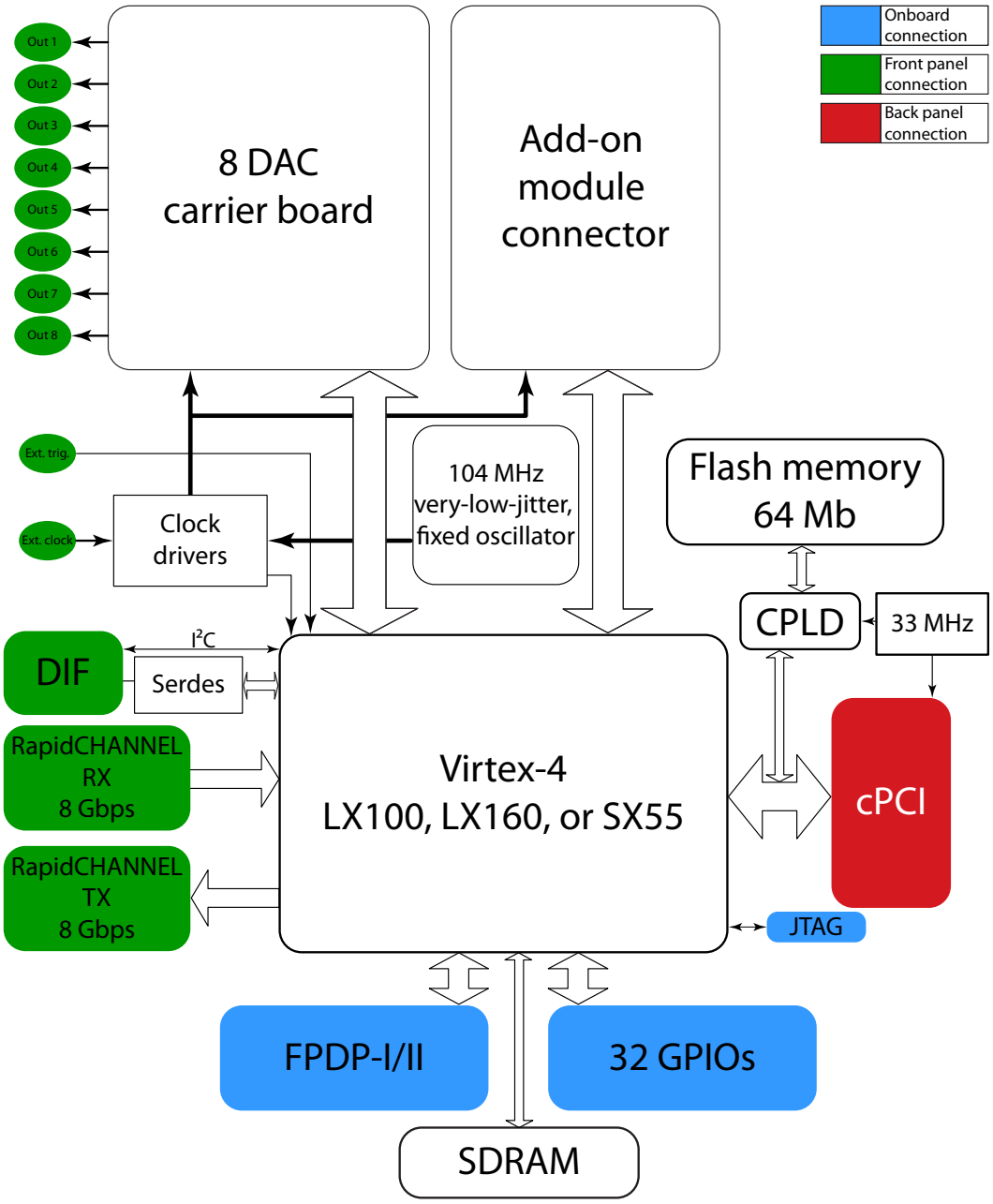
Diamond (optional)

Diamond from 3L enhances single-processor tools with a proven and simple multiprocessor model offering a level of abstraction that leads to efficient, coherent, reliable, and flexible systems. For details about this software solution, click here.

Specifications

Dual-channel digital-to-analog converters	• Texas Instruments DAC5687 (×4) • Can be upgraded to 16 channels by adding an optional add-on module • Guaranteed maximum sampling rate of 480 MSPS (resolution: 14 bits) with 4× interpolation and incoming data sample rate from the Virtex-4 FPGA of 120 MSPS (14-bit samples)	
Analog input	**Default**	50-Ω MMCX connectors
	Optional	**AC coupled** • 0.3 MHz to 240 MHz analog output bandwidth (–3 dB) • –21 dBm 2.9 dBm full-scale output (from a progammable gain min. to max.) • 83.7 dBc SFDR at an IF of 30 MHz (for a bandwidth of 50 MHz, at full scale, 4× interpolation, fine mixer, and an F_s of 416 MHz) • 88.2 dBc SFDR at an IF of 70 MHz (for a bandwidth of 30 MHz, at full scale, 4× interpolation, fine mixer, and an F_s of 416 MHz) • 89.2 dBc SFDR at an IF of 150 MHz (for a bandwidth of 30 MHz, at full scale, 4× interpolation, fine mixer, and an F_s of 480 MHz) • Interchannel crosstalk insulation of –91 dB at 30 MHz F_{out} and –82.5 dB at 70 MHz IF_{out} • SNR of 63.7 dB at 30 MHz IF_{out} and 55.2 dB at 70 MHz IF_{out}
		DC coupled • DC to 240 MHz analog output bandwidth (–3 dB) • –24 dBm to 0 dBm full-scale output (from a progammable gain min. to max.) • 84.5 dBc SFDR at an IF of 30 MHz (for a bandwidth of 50 MHz, at full scale, 4× interpolation, fine mixer, and an F_s of 416 MHz) • 87.5 dBc SFDR at an IF of 70 MHz (for a bandwidth of 30 MHz, at full scale, 4× interpolation, fine mixer, and an F_s of 416 MHz) • 87 dBc SFDR at an IF of 150 MHz (for a bandwidth of 30 MHz, at full scale, 4× interpolation, fine mixer, and an F_s of 480 MHz) • Interchannel crosstalk insulation of –83.5 dB at 30 MHz F_{out} and –82.5 dB at 70 MHz IF_{out} • SNR of 53.3 dB at 30 MHz IF_{out} and 52.3 dB at 70 MHz IF_{out}
Sampling clocks	• Software-selectable onboard or external clock • Factory-fixed oscillator, 104-MHz very-low-jitter clock (0.5 ps typical) • External 50 Ω clock source (TTL, LVTTL, CMOS, LVCMOS) used for very-low-jitter and user-defined frequencies	
Control and processing FPGA	• Processing Virtex-4 FPGA (for signal up-conversion, interpolation, and/or generation) • FPGA packages: XC4VSX55, XC4VLX100, or XC4VLX160 • 128 MB SDRAM	
Off-board communication channels	• Two RapidCHANNEL ports (TX ×1, RX ×1), yielding 8 Gbps, full-duplex • Transfers at 400 MBps through the external FPDP-I /II (software-selectable as input or output) • LVDS hardware serdes input/output DIF connection (105 MBps) on RJ45. 16-bit parallel data routed to the FPGA (serdes), 52.5 MHz maximum clock • 32-bit, PCI, external port with 33 MHz control interface • 32-bit, user-defined, external Virtex-4 single-ended GPIO-32 header • I^2C interface for stand-alone control (flash memory programming, parameter control)	
Optional add-on hardware modules Sold separetely. Contact Lyrtech for details.	**DAC module**	Eight DAC outputs, each capable of a maximum 480 MSPS (14-bit interpolating DAC) Same analog output options as the VHS-DAC
	Memory module	module adding 2 GB of DDR2 SDRAM to the VHS-DAC, yielding a solution with eight full-speed simultaneous channels for recording/playback.

Block diagram



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