



Description

This highly optimized core is designed for an OEM customer targeting Sundance DSP's DSP464 , a 4 channel ADC PMC/XMC module with an SX95T FPGA. The digitized data for all 4 channels go through four DDC cores and after certain other operation are passed to a device in real-time. The whole capture and processing is continuous and without loss of any data frames.

The DDC core can be supplied as VHDL or as a Diamond FPGA task, which could be used in conjunction with other

cores from Sundance DSP or third parties.

Features

1. input resolution: 16 b
2. Input sample rate: 81.92MHz or as specified by the application
3. DDS frequency resolution: 0.3Hz, runtime-selectable
4. SFDR: $>=84$ dB
5. Decimation: 16x fixed ,performed with cascaded CIC and Polyphase FIR filters
6. Passband Ripple < 0.2 dBpp
7. Passband width: TBD, $>= 0.4$ x output sample rate
8. Stopband attenuation, >75 dB
9. Stopband frequency: as specified by application
10. Gain: 8 power-of-2 steps, runtime-adjustable, between CIC and p-FIR
11. Rounding: bias-free convergent
12. Output resolution: 16b complex samples (16b I + 16b Q)

FC130-DDC is a complete module that includes:

- Netlist file, or VHDL source code available for additional charge
- 3L Diamond/FPGA integration support (.fcd, _pkg.vhd files) and example implementations
- VHDL testbench (requires Active-HDL or equivalent simulation environment)
- User's Guide
- C Simulation Model (available on request)
- MATLAB Simulation Model and PARS model under Simulink (available on request)



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